

AUTONETICS

A DIVISION OF NORTH AMERICAN ROCKWELL CORPORATION



HONEYWELL

EI-85

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_07531

MODEL EI-85
DIGITAL MULTIMETER

DRAWING INDEX

Nomenclature	Schematic
Switch Logic Board	115-110
Outside Power Supply Board	115-121
Decade & Symbol Board	115-122
Decade & Nixie Board	115-123
Guard Crossing	115-120
Inside Power Supply Board	115-127
Sequencer Board	115-128
Decade 10^3 & 10^4 Board	115-129
Decade 10^0 & 10^1 & 10^2 Board	115-130
Clock Board	115-131
Program Logic Board	115-132
Range Logic Board	115-133
Bridge Board	115-134
Input Function & Range Switching Board	115-148
RS-10 Board	115-143
GPA-1 Board	510-100
Null Detector Board	115-137
Outside Wiring Diagram	115-116
Inside Wiring Diagram	115-117
Inside Logic	115-149
Outside Logic	115-150
Models 85-00-13, (1), (2), (3)	
Ohms Board	115-148
AC Converter Board	115-144

TABLE OF CONTENTS

Paragraph No.		Page No.
	SECTION I - DESCRIPTION	
1.1	Introduction	1.1
1.2	Accessories	1.2
1.3	Functions	1.3
1.4	Applications	1.3
1.5	Features	1.4
1.5.1	Features included in standard meters	1.4
1.5.2	Alternate Provisions	1.5
1.6	Description	1.5
1.6.1	Front Panel Controls and Features	1.5
1.6.2	Rear Panel Connectors and Features	1.8
1.6.2.1	Signal and Reference Input Connectors	1.8
1.6.2.2	Remote Connectors J-101, J-102, and J-103	1.8
1.6.2.3	Power Input Connector and Cable	1.9
1.6.2.4	Fuses	1.9
1.7	Specifications	1.9
1.7.1	General	1.9
1.7.2	Isolation Parameters	1.10
1.7.3	DC Voltage Specifications (with preamplifier accessory)	1.10
1.7.4	DC/DC Ratio Specifications	1.11
1.7.5	DC and Ratio Operation with Filter	1.12
1.7.6	AC Specifications	1.12
1.7.7	Resistance Specifications	1.13
1.7.8	Electrical Program Inputs	1.14
1.7.9	Electrical Outputs	1.15
	SECTION II - OPERATION	
2.1	Inspection	2.1
2.2	Installation	2.1
2.3	Operating from a 220V AC Power Source	2.1
2.4	Input Connections and Grounding Considerations	2.2
2.5	Connection To External Source	2.2
2.6	Turn On and Warmup Procedure	2.4
2.7	Checkout Procedure	2.4
2.8	Operation By Front Panel Controls	2.7
2.9	Operation With a Digital Printer	2.9
2.10	Operation By Remote Control	2.10
2.10.1	Single Encoding	2.10
2.10.2	Pre-Programming	2.11
2.11	Alternate Methods of Operation	2.17
2.11.1	Pre-Programming Jumper	2.17

Table of Contents (Continued)

Paragraph No.		Page No.
	SECTION III - THEORY OF OPERATION	
3.1	Circuit Symbology and Notation	3.1
3.2	Definitions	3.1
3.3	Principle Of Operation - General	3.2
3.4	Unguarded Program and Control Logic	3.4
3.4.1	Front Panel Switching	3.5
3.4.1.1	Single Encoding	3.5
3.4.1.2	Continuous Encodings	3.9
3.4.1.3	Variable Encodings	3.9
3.4.1.4	Missing Pulse Detector	3.9
3.4.2	Remote Programming	3.10
3.4.2.1	Single Encoding	3.10
3.4.2.2	Pre-programming	3.10
3.4.2.3	Guard Crossing	3.11
3.5	Signal Conditioning Circuitry	3.11
3.5.1	Input Function and Range Switching	3.11
3.5.2	Input Buffer and Active Filter	3.13
3.5.3	AC Converter	3.15
3.5.4	Pre-Amplifier and Ohms Amplifier	3.17
3.5.4.1	Ohms Converter	3.19
3.5.4.2	Pre-Amplifier	3.21
3.5.4.3	Temperature Compensation Circuits	3.21
3.6	Reference Feedback Circuitry	3.22
3.6.1	Precision Reference Supply	3.22
3.6.2	Digital to Analog Converter	3.23
3.7	Null Detector and Control Line Circuitry	3.23
3.7.1	Null Detector	3.23
3.7.2	Control Line Circuitry	3.27
3.8	Guarded Program and Control Logic	3.27
3.8.1	Program Control and Delay	3.27
3.8.2	Program Logic and Relay Drivers	3.30
3.8.3	Sequence Delay Logic and Associated Circuits	3.30
3.9	Sequencer	3.33
3.9.1	Hi-Lo Limit Interrogation (S-1 through S-3)	3.37
3.9.2	Downranging, Polarity Reversal, and Upranging (S-4 through S-8 and S-14)	3.44
3.9.2.1	Downranging (S-4 and S-5)	3.46
3.9.2.2	Polarity (S-5 and S-6)	3.47
3.9.2.3	Upranging (S-6 through S-8)	3.47
3.9.2.4	Downrange (S-14)	3.49
3.9.3	Measurement (S-9 through S-30)	3.50
3.9.4	Reset Unguarded Register, Transmit to Unguarded Section, and Print (S-31 thru S-33)	3.53

Table of Contents (Continued)

Paragraph No.		Page No.
3.9.4.1	Guard Crossing	3.53
3.9.4.2	Transmit Program Information	3.53
3.9.4.3	Transmit Measurement Information	3.54
3.9.5	End of Sequence (S-34 through S-36)	3.54
3.10	Guarded Register	3.54
3.11	Unguarded Register	3.56
3.12	Nixie Drivers and Readout	3.61
3.12	Power Supplies - Guarded and Unguarded Sections	3.61
	SECTION IV - CALIBRATION	
4.1	Checkout Procedure	4.1
4.2	Calibration Procedure (DC and Ratio)	4.6
4.2.1	Test Equipment Required	4.6
4.2.2	Absolute Calibration	4.6
4.2.3	Preamplifier Adjustments (1V Range)	4.6
4.2.4	Preamplifier Adjustment (.1V Range)	4.8
4.2.5	Input Attenuator Adjustments	4.9
4.2.6	Ratio Calibration	4.9
4.2.7	Linearity Check and Calibration of Bridge	4.10
4.3	Calibration Procedure (AC)	4.10
4.3.1	Equipment Required	4.12
4.3.2	Zero Adjustments	4.14
4.3.3	AC Range Adjustments	4.17
4.4	Calibration Procedure (Ohms)	4.18
4.4.1	Test Equipment Required	4.18
4.4.2	Ohms Calibration	4.18

LIST OF ILLUSTRATIONS

Figure No.		Page No.
1.1	Outline Drawing (Approximate Dimensions for Planning Purposes Only)	1.16
2.1	Internal - External Grounding Configuration (Top View)	2.3
2.2	Input Connections, using standard shielded cables and banana plug connectors	2.3
2.3	Typical Signal Input Connections for Measuring DC Volts	2.5
2.4	Typical Signal Input Connections for Measuring DC/DC Ratio	2.5
2.5	Typical Signal Input Connections for Measuring AC Volts	2.6
2.6	Typical Input Connections for Measuring Resistance	2.6
2.7	Typical System Configuration for Meter "Time Sharing" Operation	2.16
2.8	Time Distribution in System Operation (Preprogramming Mode)	2.18
2.9	Preprogramming Jumper (Outside Power Supply and Control Logic Board)	2.20
2.10	Autofilter DC A Range Jumper (Range and Function Board)	2.20
3.1	Block Diagram	3.6
3.2	Unguarded Program and Control Logic	3.7
3.3	Input Function and Range Switching	3.12
3.4	Simplified Diagram, Input Buffer and Null Detector	3.14
3.5	Simplified Diagram AC Converter	3.16
3.6	Simplified Diagram of Preamplifier and Ohms Amplifier	3.18
3.7	Four-Wire Resistance Measurement	3.19
3.8	Temperature Compensation Bridge	3.21
3.9	Simplified Diagram of Precision Reference Supply and Buffer Amplifier (Inverting/Non-inverting)	3.24
3.10	Simplified D/A Converter Bridge Diagram	3.25
3.11	Control Line Circuitry	3.28
3.12	Guarded Program and Control Logic and Sequence Delay Waveforms	3.31
3.13	Relay Drivers, Range and Function Logic	3.32
3.14	Sequencer and Sequencer Output Gates	3.35
3.15	Timing Relationship of Sequencer Logic and Sequencer Output Pulses	3.36
3.16	Timing Relationship of Initial Hi-Lo Limit Interrogation (S-1 through S-3)	3.40

List of Illustrations (Continued)

Figure No.		Page No.
3.17	Hi-Lo and Threshold Logic	3.43
3.18	Timing Relationship of Ranging and Polarity Logic (S-4 through S-8)	3.45
3.19	Set Line and Reset Line	3.51
3.20	Timing Relationship of Clock Circuits and Measurement Sequence (E_x = +3.7000V)	3.52
3.21	10^4 and 10^3 Decades in Guarded Section	3.58
3.22	10^2 Decade, Logic and Waveforms (Total Count = Decimal 7)	3.59
4.1	Precision DC Source Input Connections for Checking DC Volts Measurements	4.2
4.2	Precision Potential Divider Input Connections for Checking DC/DC Ratio Measurements	4.2
4.3	Setup for Checking AC Volts Measurements	4.3
4.4	Setup for Checking Resistance Measurements	4.3
4.5	Location of Test Points and Calibration Adjustments	4.7
4.6	Location of AC Converter Adjustments and Test Points (Board 19)	4.13
4.7	Typical Setup Using Thermal Transfer Voltmeter for AC Calibration	4.16

LIST OF TABLES

Table No.		Page No.
2.1	Pin Connections for Connector J-101	2.12
2.2	Pin Connections for Connector J-102	2.13
2.3	Pin Connections for Connector J-103	2.14
2.4	Output Recording Devices and Recording Times	2.19
3.1	Program Logic and Word Designations	3.8
3.2	Current and Power Dissipation in Test Resistance	3.20
3.3	Relay Chart	3.34
3.4	Logic Level Input Requirements for Sequencer Output Gates (Negative True Logic)	3.38
3.5	Sequence of Events	3.39
3.6	Binary to Decimal Conversion Chart for the Guarded Register	3.57
3.7	Binary to Decimal Gating Logic for Unguarded Register (Any Decade)	3.60
3.8	Symbol and Decimal Point Logic for Unguarded Register	3.60
4.1	Transfer Points	4.11

SECTION I

DESCRIPTION

1.1 INTRODUCTION

The Model EI-85 Digital Multimeter is a floated and guarded, five-digit successive approximation analog-to-digital converter, designed to provide highly accurate measurements of DC volts, DC/DC voltage ratios, AC volts, and resistance. The instrument has an effective common mode rejection of more than 130 db at 60 Hz. This has been achieved by a box-within-a-box type of construction for the entire measuring section of the meter.

The instrument uses a null balance potentiometer, the most stable and accurate of all measuring techniques, to compare the unknown signal with an internal reference voltage. The internal reference voltage remains stable to 100 ppm for any consecutive six month period.

High input impedance is maintained at all times by a precision direct coupled buffer amplifier, characterized by low zero drift and a theoretically infinite input impedance. The potentiometric buffer amplifier provides for input impedances greater than 10^9 ohms on the 0.1, 1.0, and 10.0 volt ranges.

Programming, as well as transmission to the readout section of the meter, is accomplished in parallel, providing a substantial increase in operational speed as compared with similar instruments, where communication is by means of serial pulses. Communication to and from the measuring section of the meter is performed by means of a unique parallel guard crossing system.

The instrument is a five-digit meter with a resolution of 10 microvolts. A built-in normal mode filter has 60 db rejection at 60 Hz and settles to 0.001% in 500 milliseconds.

A wide variety of operational features are provided (see paragraph 1.5). As a laboratory meter, operation is accomplished by means of front panel controls. For system use, remote connectors on the rear panel provide appropriate input-output connections. Encoding rates are manually variable within time limits suitable for bench operation; a maximum rate of approximately 100 measurements per second is provided for system applications. Print level outputs are retained in storage between and during encodings so that system time sharing can be utilized. The print level outputs are supplied in both 10-line decimal and BCD formats for use in conjunction with an external printer or similar output device. The BCD outputs are in 2*421 (positive true), 8421 (positive true), or 8421 (negative true), as specified at the time of ordering.

The BCD code can be changed at a later time by replacing the decade boards with boards wired for the desired code. Solid state circuitry is used throughout the meter to assure maximum reliability with a minimum of maintenance time. All high speed switching is by transistor switches. Electro-mechanical relays are only used for infrequent changes of function, mode, range, and polarity. Etched plug-in boards containing all of the control circuitry are accessible behind the hinged front panel; lever-type extractor handles provide for easy removal and insertion.

1.2 ACCESSORIES

The standard Model EI-85 measures DC voltage (up to 1000V) and DC/DC voltage ratios (up to 100). Accessories are available to permit the measurement of AC signals (up to 750V peak at frequencies up to 100 KHz), measurement of resistance (up to 10 megohms), and operation with preamplifier (resolution of one microvolt). All accessories fit within the basic 5-1/4" chassis and may be ordered with the instrument, or added later in the field. Model number designations and accessory numbers are listed below:

Instrument Model Number	Accessories	Functions
EI-85	None	DC, Ratio
EI-85-1	1	DC, Ratio, Ohms
EI-85-2	2	DC, Ratio, AC
EI-85-3	3	DC, Ratio, Preamp
EI-85-12	1 and 2	DC, Ratio, Ohms, AC
EI-85-23	2 and 3	DC, Ratio, AC, Preamp
EI-85-123	1, 2 and 3	DC, Ratio, AC, Preamp, Ohms

When accessories are included with the instrument at the time of ordering, the instrument model number is as designated above. If it is desired to order an accessory later for installation in the field, the accessory part number should be included with the purchase order. Accessory part numbers are listed below:

Accessory Number	Nomenclature	Part Number
1	Ohms Converter	85-00-1
2	AC Converter	85-00-2
3	Preamplifier	85-00-3
13	Combination Ohms Converter and Preamplifier	85-00-13

1.3 FUNCTIONS

Operational modes and input ranges are given below. Maximum signal inputs for each range are 99999 (with appropriate decimal point), except for the AC mode where the maximum input signal in the 1KV range is 530V RMS. Autoranging and automatic filter selection (where applicable) are provided. The decimal point placement and appropriate symbol (+, -, R, ~ , K and Millivolts) are displayed with the 5 digit measurement readout.

MODES	RANGES
DC	.1V (with Accessory 3)
	1V
	10V
	100V
	1KV
RATIO	.1
	10
	100
AC (with Accessory 2)	1V
	10V
	100V
	1KV
OHMS (with Accessory 1)	1K
	10K
	100K
	1M
	10M

1.4 APPLICATIONS

The meter can readily be employed as a general laboratory instrument or as part of a system. The use of the instrument in combination with various transducers produces measurements of such quantities as temperature, pressure, weight, acceleration, or velocity in addition to direct measurements of AC and DC voltage, ratio, or resistance. System applications include automatic ground checkout of aircraft, missile, and spacecraft; automatic production line quality control; data acquisition; etc.

1.5 FEATURES

1.5.1 Features included in standard meters:

a. Measurements are displayed at the end of encodings; no fluctuating or erroneous indications are present in the readout during the encodings. Each display is held until the following encoding is completed, at which time the display is reset and the new measurement is inserted in the readout.

b. The measuring circuits of the instrument are isolated from the signal input leads by a precision potentiometric direct-coupled buffer amplifier. High input impedance is maintained at all times by the buffer amplifier, characterized by very low zero drift and a theoretically infinite input impedance. The buffer amplifier is also used as a X10 pre-amplifier to provide 10 microvolts resolution as a standard range on the basic meter (without accessories).

c. An ENCODE lamp on the front panel is illuminated when a read cycle or encoding is in progress. Since the readout does not change for repeated readings of a constant source, this feature indicates that the sampling operations are in progress.

d. The program (mode, range and filter selection) is established in the internal program logic at the start of each encoding. Since the measurement and readout sections of the meter are separated, this ensures that the correct program is included with each measurement.

e. The filter is automatically selected in the AC and ohms modes (all ranges) and in the DC mode (.1V and 1V ranges) regardless of the filter program. In the DC mode (other ranges) and in the ratio mode, the filter must be programmed either in or out by the front panel FILTER switch or by remote contact closure.

f. Incompatible programs are automatically corrected. If, for example, a range is remotely chosen that is not normally provided in the selected mode, the internal program logic automatically selects a proper range for that mode.

g. The signal input terminals open automatically and present infinite impedance to the signal source when power to the meter is removed. This protects the meter from being damaged by excessive signal magnitudes that are above the range setting.

1.5.2 Alternate Provisions

a. By removing a jumper (paragraph 2.11.1), the instrument can be pre-programmed in remote operation, i.e. the programming and sequence actions of the meter can be controlled separately by remote commands so that the time sharing technique can be incorporated into system applications. Pre-programming does not change the state of the electrical outputs containing the measurement information for the previous encoding.

1.6 DESCRIPTION

Measurements are displayed by means of Super Nixie tubes mounted in a three-position tiltable readout and consist of the measurement value, decimal point, and appropriate symbol or polarity sign. Controls are identified on the panel; concentric controls are color-coded, red and black, corresponding to the color of the corresponding placarded positions.

1.6.1 Front Panel Controls and Features

POWER switch:	OFF removes AC power and disconnects the signal inputs to the instrument
	ON places the meter in full operation (readout illuminated indicates the presence of AC power)
ENCODE switch:	SINGLE (springloaded position) selects one measurement cycle and printout
	CONT provides for continuous encodings at a rate variable by the VAR ADJ control
	RMTE provides for remote programming

NOTE

See specifications, paragraph 1.7 for encoding rates.

VAR ADJ Control:	Adjusts the encoding rate when the ENCODE switch is set to the VAR position.
ENCODE lamp:	Illuminates during each read cycle or encoding.
RANGE Switch:	AUTO provides for automatic ranging. RMTE provides for remote programming of range. The manual range positions select ranges applicable to the measurement mode: RATIO, DC, AC or OHMS. Guide lines to the MODE switch indicate the set of ranges that apply. Ranges and input signal limitations for each mode are listed below.

NOTE

In automatic range operation, the meter downranges for any signal value less than 1 (most significant decade) to allow for a maximum number of digits resolution. The meter upranges at 99999.

DC VOLTS MODE

RANGE	AUTO	MANUAL
.1V	±00.000MV to ±99.999MV	±00.000MV to ±99.999MV
1V	±.10000V to ±.99999V	±.00000V to ±.99999V
10V	±1.0000V to ±9.9999V	±0.0000V to ±9.9999V
100V	±10.000V to ±99.999V	±00.000V to ±99.999V
1 KV	±100.00V to ±999.99V	±000.00V to ±999.99V

DC/DC RATIO MODE

RANGE	AUTO	MANUAL
1	R.00000 to R.99999	R.00000 to R.99999
10	R1.0000 to R9.9999	R0.0000 to R9.9999
100	R10.000 to R99.999	R00.000 to R99.999

AC VOLTS MODE

RANGE	AUTO	MANUAL
1V	.00000V to .99999V	.00000V to .99999V
10V	1.0000V to 9.9999V	0.0000V to 9.9999V
100V	10.000V to 99.999V	00.000V to 99.999V
1 KV	100.00V to *750.00V	000.00V to *750.00V

OHMS MODE

RANGE	AUTO	MANUAL
1K	.00000K to .99999K	.00000K to .99999K
10K	1.0000K to 9.9999K	0.0000K to 9.9999K
100K	10.000K to 99.999K	00.000K to 99.999K
1M	100.00K to 999.99K	000.00K to 999.99K
10M	1000.0K to 9999.9K	0000.0K to 9999.9K

MODE Switch: AC, DC, RATIO, and OHMS positions select the corresponding instrument modes

RMTE provides for remote programming of mode

FILTER Switch: OUT removes the built-in 60 db filter from the signal input circuit

IN inserts the built-in 60 db filter into the input circuit

RMTE provides for remote programming of filter.

READOUT:	The Super Nixie readout consists of five digits, five decimal points, and the following symbols:	
	DC mode:	+ or - (polarity changes automatically)
	DC/DC ratio mode:	The letter R
	AC mode:	The symbol ~
	OHMS mode:	The letter K
MILLIVOLTS Lamp:	Illuminates when the meter is in the DC mode, .1V range	

*Maximum signal input voltage in AC mode is 530 volts RMS.

1.6.2 Rear Panel Connectors and Features

1.6.2.1 Signal and Reference Input Connectors

Five binding posts on the rear panel are identified from left to right as follows:

HI (red) is the input jack for the high side of the signal input.

LO (red) is the input jack for the low side of the signal and/or external reference input.

GUARD (silver) is the shielded guard connection.

REF (red) is the input jack for the high side of the external reference or ohms reference.

OHMS (black) is the input jack for ohms measurement.

NOTE

See Figure 2.6 for ohms input connections.

1.6.2.2 Remote Connectors J-101, J-102, and J-103

Remote Connectors J-101, J-102, and J-103, located on the rear panel, provide the input/output connections for remote programming, 10 line decimal print level outputs and binary coded outputs in either 8421 or 2*421 code. See Tables 2.1, 2.2, and 2.3 for input/output connections.

1.6.2.3 Power Input Connector and Cable

The power input connector J-104 is a three terminal jack with a chassis ground connection. The power cable is fitted with a mating plug for connection to the instrument and is terminated with a standard three prong plug for connection to the power source.

1.6.2.4 Fuses

Both sides of the AC power input are fused. Two 2 ampere 3 AG slo-blo fuses for 110V operation, or two 1 ampere 3 AG slo-blo fuses for 220V operation are located next to the power input connector on the rear panel.

1.7 SPECIFICATIONS

1.7.1 General

Instrument Type:	Successive approximation, full floating and guarded, differential
Display:	Six window Burroughs Super long-life Nixie with orange circularly polarized filter
Power Requirements:	105 to 125 volts AC, or 210 to 250 volts AC (label on rear panel shows correct voltage rating) -150 watts or less
Frequency of Power Source:	60 Hz ±20% (instrument can be ordered for 400 Hz, ±20% operation)
Relative Humidity:	To 80%
Dimensions (see Figure 1.1):	
Weight:	Approximately 45 lbs.
Mounting Position:	Rack or table (Model 6505 Portable Case can be ordered separately)
Warmup Time:	30 minutes at ambient temperature
Design Limits:	
Storage Temperature:	-20° C to +85° C
Humidity:	0 to 98%
Pressure:	Sea level to 50,000 feet

1.7.2 Isolation Parameters:

Maximum Operating Voltages:

Guard to Power Ground:	500 volts peak-to-peak AC or 500 volts DC
Guard to High Side:	1000 volts peak to peak
Guard to Low Side:	1000 volts peak to peak
Common Mode Rejection:	130 db at 60 cps, unfiltered, with up to 100 ohms unbalance in either lead
	160 db at 60 cps, filtered, with up to 1000 ohms unbalance in either lead

1.7.3 DC Voltage Specifications (with preamplifier accessory)

Ranges:	Range Letters:	Auto		Manual	
.1V	A'	±00.000MV	to ±99.999MV	±00.000MV	to ±99.999MV
1V	A	±.10000V	to ±.99999V	±.00000V	to ±.99999V
10V	B	±1.0000V	to ±9.9999V	±0.0000V	to ±9.9999V
100V	C	±10.000V	to ±99.999V	±00.000V	to ±99.999V
1KV	D	±100.00V	to ±999.99V	±000.00V	to ±999.99V

Automatic Features:

Accuracy, ASA Reference Conditions (23° C ±1° C, 7 hours)

Range Full Scale	Accuracy
99.999MV	±.01% of reading ±.005% full scale
.99999V	±.01% reading ±.002% full scale
9.9999V	±.005% reading ±.001% full scale
99.999V	±.005% reading ±.001% full scale
999.99V	±.005% reading ±.001% full scale

Accuracy, ASA Rated Conditions (12° C to 40° C)

Range Full Scale	Accuracy
99.999MV	±.02% reading or ±.01% full scale
.99999V	±.015% reading or ±.01% full scale
9.9999V	±.01% reading or ±.002% full scale
99.999V	±.01% reading or ±.002% full scale
999.99V	±.01% reading or ±.002% full scale

Step Response: 10 milliseconds read time

Delay Times for Each Range and Polarity Change: 20 milliseconds

NOTE

Range, Polarity and Step Response Delay Times are increased to 500 milliseconds in the .1V and 1.0V Ranges.

Ranging Points: Uprange at 99999
Downrange at 10000

In put Impedance: Potentiometric input buffer amplifier provides full time source unloading on .1V, 1V, and 10V ranges

10 megohms in 100V and 1KV

Maximum Signal Input Voltage: 999.99V

1.7.4 DC/DC Ratio Specifications

Ranges:	Range Letters:	Auto	Manual
1	A	R.00000 to R.99999	R.00000 to R.99999
10	B	R1.0000 to R9.9999	R0.0000 to R9.9999
100	C	R10.000 to R99.999	R00.000 to R99.999

Automatic Features: Ranging and Polarity

NOTE

Polarities of signal and reference voltages can be positive or negative, but must be in the same polarity.

Accuracy, ASA Rated Conditions (12°C to 40°C):
±.003% reading ±10/E_{ref} .001% full scale

Reference Voltage: 11V maximum

Step Response and Delay Times: Same as for DC

Program Time: 250 milliseconds internal delay for initial function change.

Signal Input Impedance: Potentiometric in 1 range; 10 megohms in 10 and 100 ranges

Reference Input Impedance: 100 kilohms

1.7.5 DC and Ratio Operation with Filter

Normal Mode Rejection

Rejection:	60 db at 60 cps minimum
Characteristics:	Three-pole Gaussian
Cut-Off Rate:	18 db/octave
Settling Time:	500 milliseconds to .001%

Step Response: 500 milliseconds read time

Delay Time for Each Range and Polarity Change: 500 milliseconds

1.7.6 AC Specifications

Ranges:	Range Letters:	Auto	Manual
1V	A	.00000 to .99999	.00000 to .99999
10V	B	1.0000 to 9.9999	0.0000 to 9.9999
100V	C	10.000 to 99.999	00.000 to 99.999
1KV	D	100.00 to 530.00	000.00 to 530.00

Automatic Features: Ranging

Accuracy, ASA Reference Conditions

50 Hz to 10 KHz

1V and 10V:	±.02% full scale ±.05% reading
100V and 1KV:	±.02% full scale ±.1% reading

10 KHz to 30 KHz

1V and 10V:	±.03% full scale ±.1% reading
100V and 1KV:	±.03% full scale ±.3% reading

30 KHz to 100 KHz

1V and 10V:	±.1% full scale ±.3% reading
100V and 1KV:	±.1% full scale ±.5% reading

Accuracy, ASA Rated Conditions

50 Hz to 10 KHz

1V and 10V:	±.02% full scale ±.1% reading
100V and 1KV:	±.02% full scale ±.15% reading

10 KHz to 30 KHz

1V and 10V:	±.03% full scale ±.2% reading
100V and 1 KV:	±.03% full scale ±.4% reading

30 KHz to 100 KHz

1V and 10V:	±.1% full scale ±.75% reading
100V and 1KV:	±.1% full scale ±1.0% reading

Calibration:	Average reading calibrated to RMS value for sine wave input
Frequency Response:	50 Hz to 100 KHz
Step Response:	500 milliseconds read time
Delay Time for Range Change:	500 milliseconds
Ranging Points:	Uprange at 99999 Downrange at 10000
Maximum Signal Input Voltage:	530 V AC RMS

1.7.7 Resistance Specifications

Ranges:	Range Letters:	Auto	Manual
1K	A	.00000K to .99999K	.00000K to .99999K
10K	B	1.0000K to 9.9999K	0.0000K to 9.9999K
100K	C	10.000K to 99.999K	00.000K to 99.999K
1M	D	100.00K to 999.99K	000.00K to 999.99K
10M	E	1000.0K to 9999.9K	0000.0K to 9999.9K

Automatic Features:	Ranging
Resolution:	10 milliohms

Accuracy, ASA Reference Conditions

Range Full Scale	Accuracy
.99999K	±.01% reading ±.002% full scale
9.9999K	±.007% reading ±.001% full scale
99.999K	±.007% reading ±.001% full scale
999.99K	±.01% reading ±.001% full scale
9999.9K	±.02% reading ±.002% full scale

Accuracy, ASA Rated Conditions

Range Full Scale	Accuracy
.99999K	±.02% reading ±.002% full scale
9.9999K	±.01% reading ±.001% full scale
99.999K	±.01% reading ±.001% full scale
999.99K	±.03% reading ±.001% full scale
9999.9K	±.05% reading ±.001% full scale

Voltage and Current Through Unknown

10 volts full scale all ranges

Current	Range
10 milliamps	1K
1 milliamp	10K
0.1 milliamp	100K
0.01 milliamp	1M
0.001 milliamp	10M

Step Response: 500 milliseconds read time

Delay Time for Each Range Change: 500 milliseconds

1.7.8 Electrical Program Inputs

Single Encode

Positive going AC coupled edge, 6 to 12 volts peak, 10 μ seconds minimum rise time, 20 μ seconds minimum width

Range, Function and Filter Enable:

Switch (transistor or closure) or voltage state

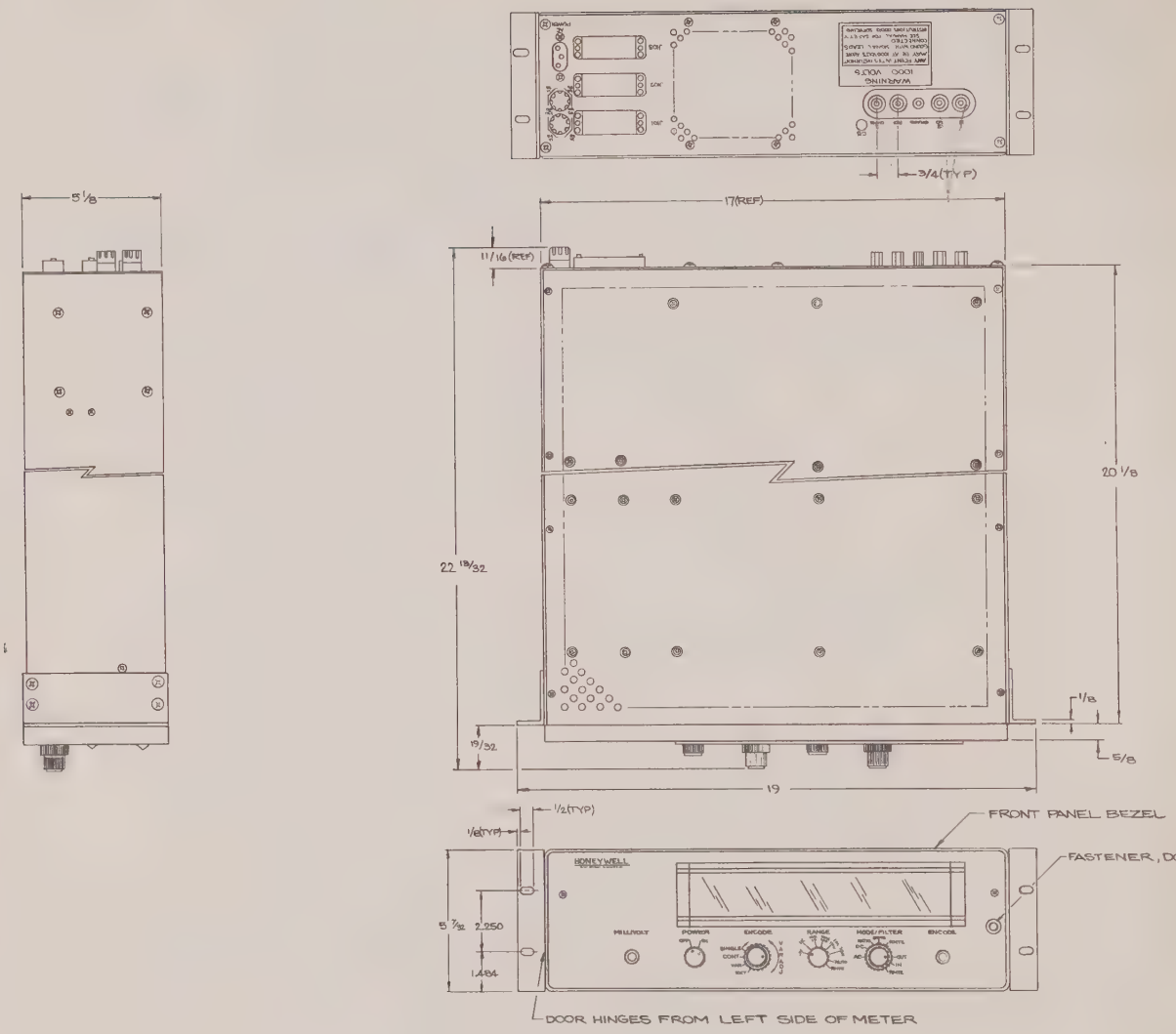
Switch: open = -12V, closed = 0V at 2 ma. The form A closure would be between appropriate remote line and desired program lines

Voltage State: "On" line = -12V at 2 ma. Voltage should be applied across desired program lines and logic ground

For range selection, 5 lines corresponding to decimal point positions are provided. For function and filter selection, 6 lines are provided.

1.7.9 Electrical Outputs

BCD Range, Function, Reading and Print Command:	Positive True 2*421 False No Load = 0 to +0.3V. 5 ma maximum load True No Load = 10V ±1V. 0.1 ma maximum load
10 Line Decimal Outputs:	False = +70V, 0.1 ma maximum load True = 0V ±2V, 1.0 ma maximum load
Decoded Range and Function Outputs:	False = +70 volts, 0.1 ma maximum load True = 0 volts ±2V, 1.0 ma maximum load



Outline Drawing (Approximate Dimensions for Planning Purposes Only)

Figure 1.1

SECTION II

OPERATION

2.1 INSPECTION

After being unpacked, the equipment should be inspected for shipping damage. If damage is found, an immediate report should be made to the shipping agency and to Honeywell Inc. If equipment fails to operate as specified, check all connectors, cables and fuses. Should the equipment fail to operate satisfactorily during the warranty period, follow the procedure outlined in the warranty.

2.2 INSTALLATION

Normally the instrument is shipped with rack mounting flanges, ready for mounting in a standard 19" instrument rack. If a portable unit is desired, a Model 6505 Portable Case can be installed at the factory or shipped separately for installation in the field.

Rack mounting is accomplished by the use of screws which pass through the two rack mounting flanges to the rack.

To mount the multimeter in the portable case, first remove the rack mounting flanges from the meter. Slip the portable case over the instrument and align the angle bracket inside the case with the tapped holes on the sides of the instrument. Secure the case to the instrument with eight 10-32x1-1/2" TR HD screws; use the holes where the rack mounting flanges previously mounted and the additional holes at the rear of the side panels. Then turn the instrument over and remove one screw from each corner of the bottom cover plate. Place spacers over the four holes and place the bottom cover of the case over these. Secure the bottom with four 6-32x1" TR HD screws passing through the rubber feet, the bottom cover, and the spacers to the bottom cover of the instrument.

2.3 OPERATING FROM A 220V AC POWER SOURCE

The instrument is normally wired for operation from a 105-125 volt AC (60 or 400 cps, ±20%) power source unless otherwise specified. However, a simple wiring change at the input to the power transformer permits operation from a 210-250 volts AC (60 or 400 cps, ±20%) source. Instructions for this modification are included in the wiring diagram (outside) at the rear of this text. To reach the transformer connections, remove four screws from the four corners of the rear panel and fold the panel back. (see note 1, Figure 1.1).

2.4 INPUT CONNECTIONS AND GROUNDING CONSIDERATIONS

Measurement circuitry is divided into two sections, guarded and unguarded; each of these is isolated from the other and from the external case. Each section is individually grounded. All signals to and from the guarded section must pass through the guard. The guard, ground, and shielding configuration is illustrated in Figure 2.1.

So that the isolation features of the meter will not be lost, the following precaution should be noted. Input cables and connectors should be adequately shielded; each shield should connect to the GUARD connector at the meter, and to the source of common mode interference at the unknown source. Figure 2.2 illustrates the recommended cable setup. Note that each line is separately shielded (guarded). In non-critical applications, the GUARD and LO input terminals may be shorted at the meter. The guard and/or low lines can safely be floated to a maximum of 500 volts above or below chassis ground.

WARNING

With signal leads connected to the meter, any common mode voltage existing between the signal source and chassis ground (earth ground) will be present between the guard, signal common, and the chassis. This presents no hazard while the front service door is closed. However, before the door is opened, either disconnect the signal leads from the meter or confirm that no hazardous common mode voltages exist at the signal source.

2.5 CONNECTION TO EXTERNAL SOURCE

Figures 2.3, 2.4, 2.5, and 2.6 illustrate typical DC, ratio, AC, and resistance sources, and the proper method of connecting the guard to eliminate common mode interference. The internal inter-layer capacitances and resistances in the meter are illustrated in the figures. The values of C1 and C2 vary considerably under various operating conditions. Both capacitances are dependent upon the length of the signal input cables and stray capacity at the multimeter and at the source. C3 is very small, less than 4 pf, and Rs is more than 10^{10} ohms. The guard provides a path for the AC and DC common mode signals, thereby shunting the current from the normal mode path and through the unbalance resistance R_{ub}.

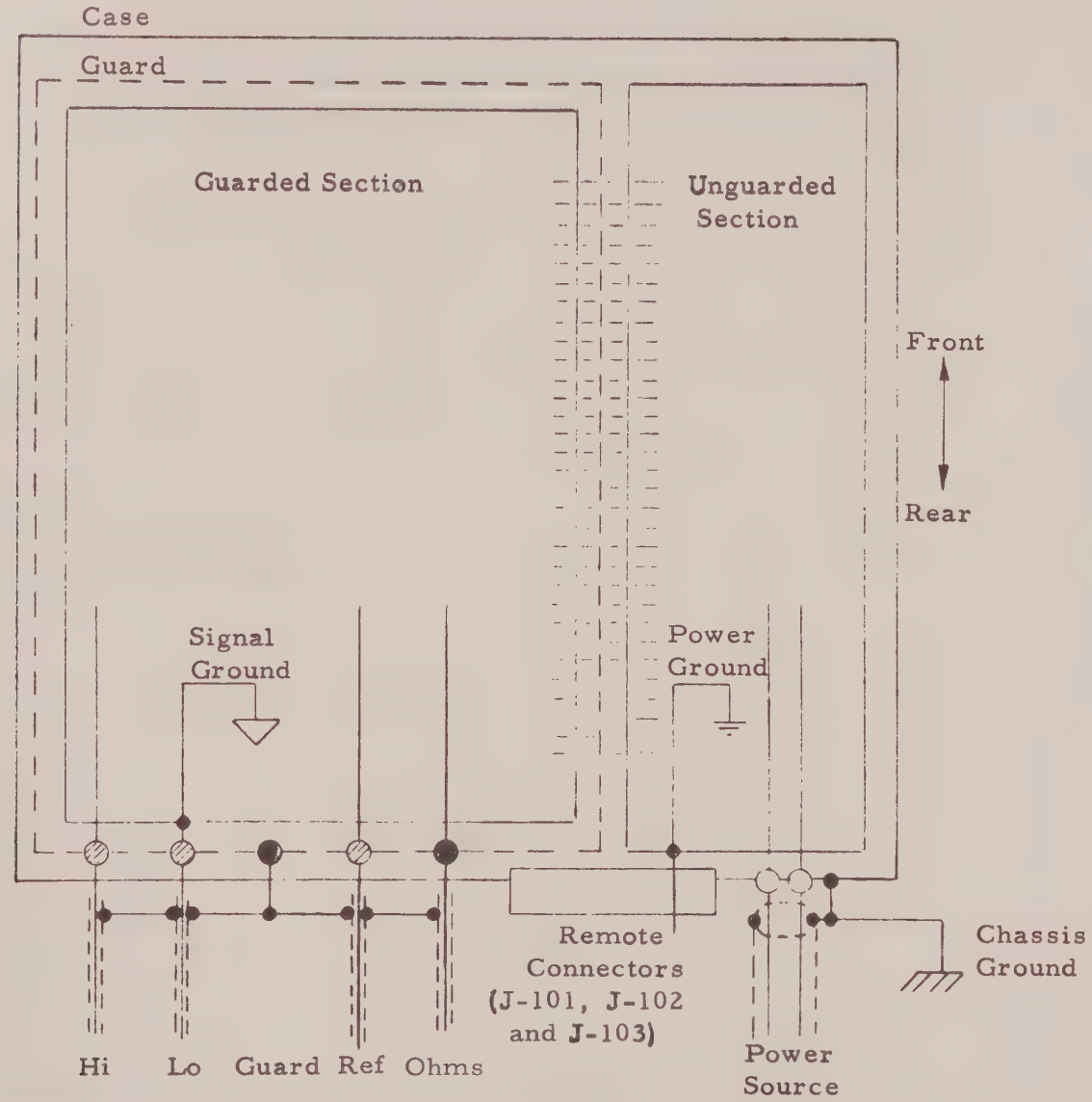


Figure 2.1. Internal - External Grounding Configuration (Top View)

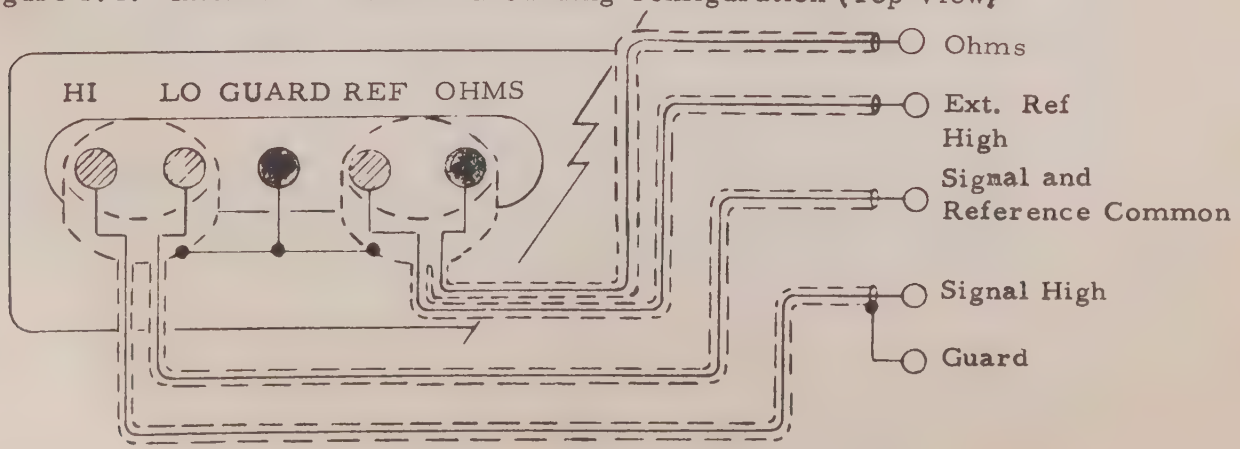


Figure 2.2. Input Connections, using standard shielded cables and banana plug connectors.

When the source of common mode voltage is connected to the guard, almost all of the common mode current flows through the guard, R2 and C2, while practically no current flows through the signal lines, R3 and C3. The unbalance between the high and low signal lines is shown as resistor R_{ub} in the high side. The effective common mode rejection of the meter is 130 db at 60 cps, based on a resistance R_{ub} of 100 ohms unbalance in the signal input lines.

In the illustrations the source of common mode interference is at the signal common line; this is generally the case in actual applications. A common mode voltage is shown between the chassis grounds. This common mode signal depends upon the distance between the two instruments and the connections to earth ground.

Situations may be encountered where the source of common mode interference is other than the common line, such as the high side of the signal line. In this case the guard would be connected to the high side.

2.6 TURN ON AND WARMUP PROCEDURE

a. With the POWER switch in the OFF position, connect the power input cable to a suitable source of AC power (see paragraph 2.2.1).

b. Connect shielded leads to the HI and LO input connectors, and REF connector (when applicable). All shields should tie to the GUARD connector.

c. If the instrument is to be used with a printer, or if it is to be operated remotely, connect cables to the appropriate connectors on the rear panel, using standard AMP 50 pin connectors or equivalent. See Tables 2.1, 2.2, and 2.3 for pin connections, and paragraphs 2.9 and 2.10 for operating instructions.

d. Set the POWER switch to ON and allow fifteen minutes warmup time. The Nixie tubes in the readout indicator will light, indicating that AC power is applied to the instrument. The numerical value in the readout has no significance at this time.

2.7 CHECKOUT PROCEDURE

A checkout procedure is included in section IV of this manual. Before initial operation, and at periodic intervals (depending on the instrument use), this procedure should be performed to ensure that the multimeter is operating within specifications.

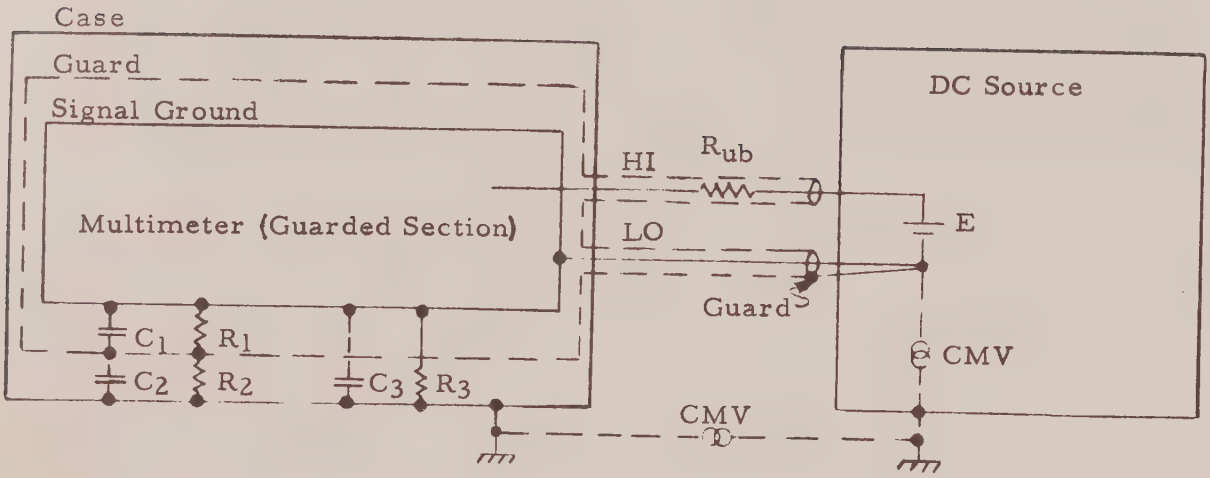


Figure 2.3 Typical Signal Input Connections for Measuring DC Volts

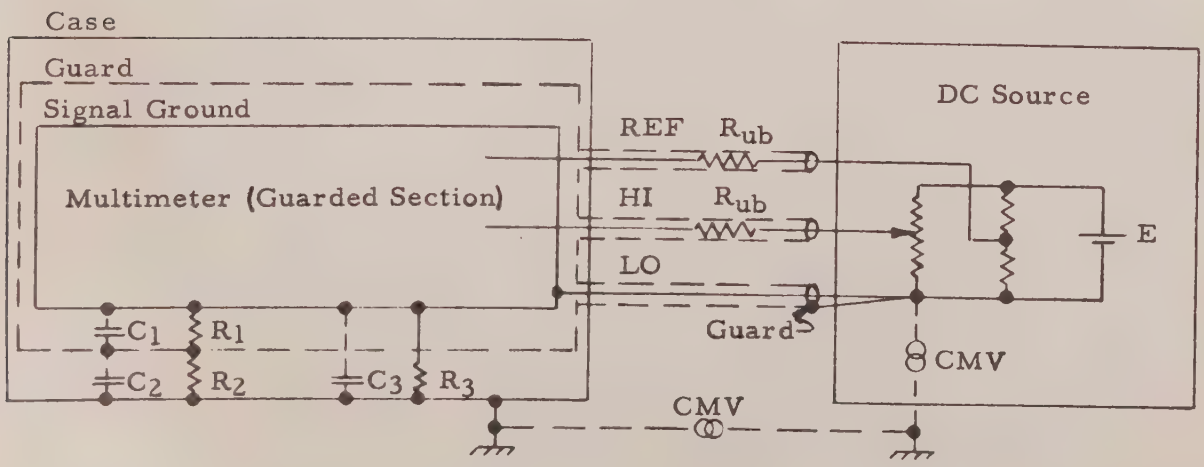


Figure 2.4. Typical Signal Input Connections for Measuring DC/DC Ratio

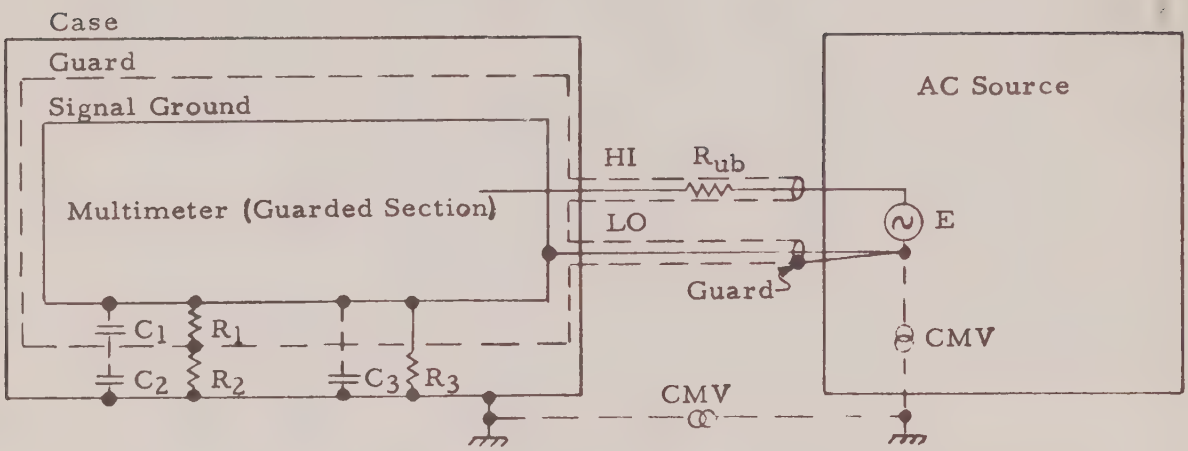


Figure 2.5. Typical Signal Input Connections for Measuring AC Volts

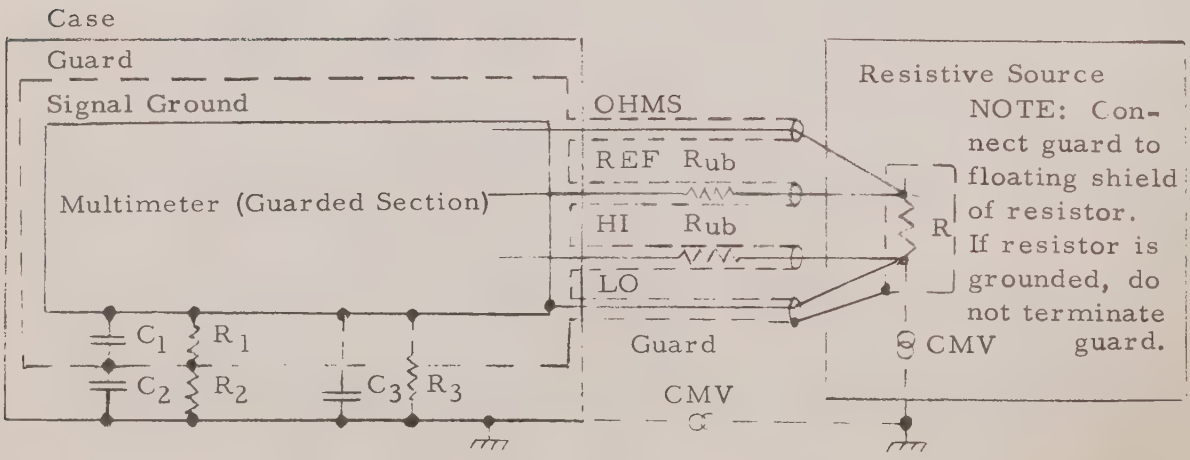


Figure 2.6. Typical Input Connections for Measuring Resistance

2.8 OPERATION BY FRONT PANEL CONTROLS

a. Perform turn on and warmup procedure outlined in paragraph 2.6.

b. Set the ENCODE switch to SINGLE

c. Set the VAR ADJ control fully counterclockwise.

d. Set the MODE switch to the setting corresponding to the type of measurement desired.

e. Set the RANGE switch to AUTO.

f. Set the FILTER switch to OUT.

g. In DC, ratio and AC modes, refer to Figures 2.3 through 2.5 for input cabling.

CAUTION

Input voltages must not exceed 1000V in the DC and ratio modes, 750V peak in the AC mode. The reference voltage must not exceed 11V in the ratio mode.

Connect the signal input cable (HI) to the high side of the input voltage, and the common cable (LO) to the low side of the input voltage. For ratio measurements, connect the reference cable (REF) to the external reference voltage and the common cable (LO) to the low side of the reference (both the signal and reference must be of the same polarity). Connect the guard to the source of common mode interference; if this is not critical, short the GUARD and LO terminals at the multimeter.

h. In OHMS mode, refer to Figure 2.6 for input cabling.

CAUTION

It is important that each lead be connected properly for ohmic measurements. To avoid errors, especially when measuring high resistance values, it is recommended that the operator employs caution with regard to shielding and guarding. If the test resistor is surrounded by a floating shield, the GUARD lead should be terminated at the shield. If the test resistor is connected to ground, the GUARD lead should not be used. There must be no voltage present across the test resistance.

Connect both the OHMS and REF cables to one side of the resistance to be measured, and connect both the HI and LO cables to the other side of the resistance. Connect GUARD as required (see CAUTION above).

i. Set the ENCODE switch to CONT. After a short delay, the readout will indicate the measurement and the appropriate symbol or polarity sign.

j. If the source or external reference (ratio mode) is unstable, or if AC noise (normal mode interference) is present, the displayed measurement magnitude will vary considerably from one encoding to the next.

k. If the guard is properly connected and the readout remains unstable, set the FILTER switch to IN (DC and ratio modes).

NOTE

When the filter is in, the program time is 500 milliseconds and each range or polarity change requires an additional 500 milliseconds.

l. The ENCODE switch should be left in the CONT position for continuous encodings at a maximum fixed rate. However, if it is desired to change the encoding rate, the ENCODE switch should be set to the VAR position and then the encoding rate can be decreased by adjustment of the VAR ADJ control in the clockwise direction. The SINGLE position of the ENCODE switch provides single encodings, and is normally used when the instrument is connected to a printer. For operation of the meter with a printer, set the ENCODE switch to the spring-loaded position and release; the printer will record the measurement at the end of the encoding.

m. Manual range selections substantially reduce the encoding time. Therefore, when the signals to be measured are expected to remain within one of the ranges of the meter, set the RANGE switch to the lowest range that exceeds the maximum measurement. This provides for the greatest resolution. An overrange indication (input signal above the range capabilites of the selected range) is an all 9's condition. When an overrange occurs, increase the setting of the RANGE switch.

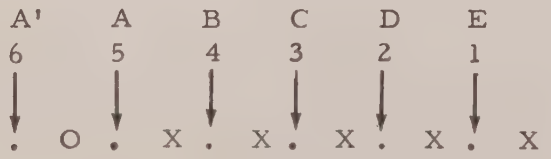
NOTE

When the RANGE switch is moved from one position to another, the decimal point in the readout will not immediately change positions. This is because front panel readout is controlled entirely from the program and measurement information contained in the guarded section, which is transferred across the guard with the readout indication and printout at the end of each encoding.

2.9 OPERATION WITH A DIGITAL PRINTER

Electrical signals are provided at connectors J-102 and J-103 on the rear panel (see Tables 2.2 and 2.3), which can be used to directly drive a Honeywell Inc. Model 9057 Digital Recorder or other output device able to accept 0 volts on the selected lines and +70 volts on non-selected lines. Information provided at the connectors includes five 10-line decimal digits representing the measurement magnitude, five symbols (+, -, R, ~ , and K) indicating the mode, and six range codes representing the decimal point placement.

Each range code can be considered as an exponent code, where negative powers of ten indicate the decimal point placement as illustrated below.



The print command is a +12 volt positive going edge from ground and is obtained from pin k, connector J-102. The meter will generate a print command for all measurements.

When the meter is used with the Model 9057 Digital Recorder, an 11 column printed format is produced as shown below. For system operation, three columns are provided for the scanner channel identification (optional).

11	10	9	8	7	6	5	4	3	2	1 ← Printwheel positions (columns)
X	X	X	X	X	X	X	X	X	X	X

Range Code
Magnitude
Symbol

Scanner Channel ID
(optional)

2.10 OPERATION BY REMOTE CONTROL

For remote operation, all front panel switches are set to the REMOTE position. The switching action of all front panel controls can then be duplicated remotely by form A contact closures from the remote lines to the desired program considerations (through connectors J-101 and J-102), except for the POWER switch and the VAR ADJ control. The encoding rate in remote operation is 100 measurements per second (maximum); range changing, polarity reversal, and filtered measurements require additional encoding time. To start each encoding or measurement sequence, a remote single encoding command or remote start command is required. The command must be delayed at least 3 milliseconds after the program has been entered into the meter to allow the program gates to be enabled.

2.10.1 Single Encoding

When the meter is operated with a printer (see paragraph 2.9), the combination can be used as a closed loop system, where the "print complete" command from the printer is routed to pin z, connector J-102, and initiates the next encoding.

Single encoding operation by remote control is accomplished by an AC coupled positive going edge. A positive going edge from pin z to pin DD connector J-102, will start an encoding.

The instrument can encode at a maximum rate of 100 measurements per second when there are no program changes and the filter is not used. At this maximum speed, the delay time is approximately 2 milliseconds and the encode time is approximately 8 milliseconds. Thus the total read time is approximately 10 milliseconds. If there are any program changes, additional delays will be required.

2.10.2 Pre-Programming

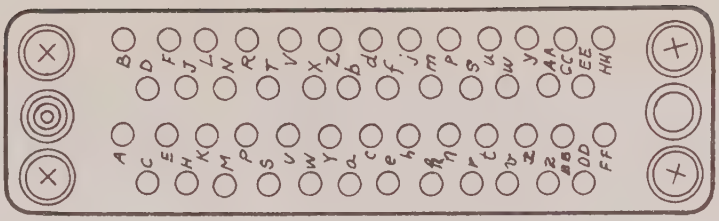
Pre-programming consists of entering the program into the meter and establishing the program in the internal program logic (relays and flip-flops) before the measurement is actually performed. Then, at a certain time (depending upon the system application) the meter encoding is started. At the end of the encoding cycle the meter generates a "print" command, controlling the printer or recording device. The "print" command from the meter and the "print complete" command from the printer or recording device are used to maintain a closed loop system.

To operate the meter in the pre-programming mode, the jumper wire on the outside power supply and control logic board must first be removed (see Figure 2.9). A remote "program transmit" command and a remote "start" command are then required for each encoding. The remote program transmit command and the remote start command must be positive going (as specified in paragraph 1.7.7). The remote program transmit command is brought into the meter between pins HH and DD (logic ground), connector J-102. The remote start command is brought into the meter between pins z and DD. Both are AC coupled.

A typical system made up from Honeywell Inc. modules is illustrated in Figure 2.7 and a corresponding timing diagram for three example input channels is shown in Figure 2.8. Similar systems can be built as long as the timing requirements for the meter are satisfied. The print time in the timing chart is for a Model 9057 Digital Recorder; alternate recording devices with their corresponding time requirements are listed in Table 2.4. The print command from the meter is used as a "step" command for the scanner. The programmer is driven by the scanner so that a new program is selected with each new channel. After a fixed delay of approximately 25 milliseconds (Model 707-600 Scanner switching time), the scanner generates a "remote programming" command. This command is routed to the meter and transmits the program across the meter guard, allowing the programming part of the cycle to commence. During this time, the program is established in the internal logic but the encoding is inhibited until an "encode" command is received. The "print complete" command from the printer is routed to the meter as an "encode" command

J-101

MODEL-85
10-Line
Magnitude
Connector

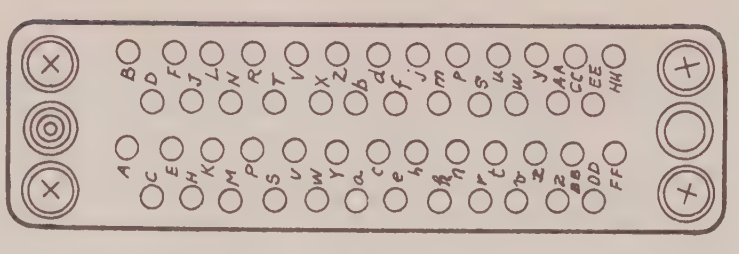


PIN		Function
B	0	
F	1	
L	2	
R	3	
V	4	10^0 Digit of Measurement
Z	5	
d	6	
j	7	
P	8	
u	9	
y		
CC		
HH		
D	0	
J	1	
N	2	
T	3	
X	4	10^1 Digit of Measurement
b	5	
f	6	
m	7	
s	8	
w	9	
AA		
EE		
A	0	
E	1	
K	2	
P	3	
U	4	10^2 Digit of Measurement
Y	5	
c	6	
h	7	
n	8	
f	9	
x		
BB		
FF		
C	0	
H	1	
M	2	
S	3	
W	4	10^3 Digit of Measurement
a	5	
e	6	
k	7	
r	8	
v	9	
z		
DD		

Table 2.1. Pin Connections for Connector J-101

J-102

MODEL-85
10^4 Magnitude Range and Symbol

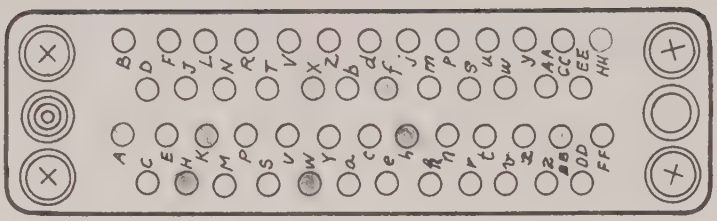


PIN		Function	
B	0		
F	1		
L	2		
R	3		
V	4	10^4 Digit of Measurement	
Z	5		
d	6		
j	7		
p	8		
u	9		
y			
CC			
HH			
D			
J	1	XXXX.X E Code	
N	2	XXX.XX D Code	
T	3	XX.XXX C Code	Range Multiplier
X	4	X.XXXX B Code	
b	5	.XXXXX A Code	Negative Exponent
f	6	.0XXXXX A' Code	
m			
s			
w			
AA			
EE			
A			
E			
K	+	Plus DC Volts	
P	-	Minus DC Volts	
U	N	AC Volts	
Y			
c			
h	K	Kilohms	
n			
t			
x	R	Ratio	
BB			
FF			
C			
H			
M			
S			
W			
a			
e			
k		Print Command	
r			
v			
z		Encode Command	
DD		Logic Ground	

Table 2.2. Pin Connections for Connector J-102

J-103

MODEL-85
BCD



PIN	"Option" for Magnitude Only		Function
B	2*	8	10^0 Decade
F	4	4	
L	2	2	
R	1	1	
V	2*	8	10^1 Decade
Z	4	4	
d	2	2	
j	1	1	
p	2*	8	10^2 Decade
u	4	4	
y	2	2	
CC	1	1	
HH			Remote Programming
D	2*	8	10^3 Decade
J	4	4	
N	2	2	
T	1	1	
X	2*	8	10^4 Decade
b	4	4	
f	2	2	
m	1	1	
s	R1	1	Range Multiplier
w	R2	2	
AA	R3	4	
EE			Print Command
A	+		Plus DC Volts
E	-		Minus DC Volts
K	N		AC Volts
P	R		Ratio
U	K		Kilohms
Y			
c			Remote Range
h			Auto
n			E Range
t			D Range
x			C Range
BB			B Range
FF			A Range
C			A' Range
H			Remote Mode
M			Ohms
S			Ratio
W			DC
a			AC
e			Remote Filter
k			Filter In
r			Filter Out
v			
z			Encode Command
DD			Logic Ground

Remote Programming Inputs

Table 2.3. Pin Connections for Connector J-103

initiating the encoding. If the "encode" command is generated before the program is completely established in the internal program logic, the command will be retained in the meter until the appropriate time and the sequence will then be initiated automatically. The timing relationship of the system is such that the meter is processing the program for one channel while the previous channel is being printed. Also, there is no overlapping of meter operations since the start of each encoding is inhibited until the previous channel is printed (see timing chart, Figure 2.8).

NOTE

If the scanner channel identification is desired to be recorded along with the meter data, storage of this information is required due to the fact that the scanner is advanced by the "print" command.

Four typical input signals with corresponding programs for the four modes of operation are used in the figure to illustrate typical combinations of channels and programs encountered in system operation. The first channel (+5.7601V) is programmed for DC, 10V range and no filter; no polarity reversal or range change is required. The second channel (R93.221) is programmed for ratio, autorange, and filter; one range change is required. Since this channel(and the following two channels) use the filter, the delay times are increased to 500 ms, with an additional 500 ms for each range change. The third channel (~.60000V) is programmed for AC, and autorange (the filter is automatically selected in the AC and ohms modes); one range change is required. The fourth channel (86,342KΩ) is programmed for ohms and autorange; two range changes are required.

Initially channel 1 is selected by the scanner and program 1 is selected by the programmer. Both are routed to the meter. To start the system a "remote programming" and an "encode" command must be generated externally by the operator. The "encode" command should be generated a few milliseconds after the "remote programming" command. The "remote programming" command transmits program 1 across the meter guard to the internal program logic. If the "encode" command is received by the meter before the programming is complete, the command will be retained in the meter until the appropriate time and the encoding for channel 1 is then begun.

At the end of the encode cycle for channel 1, a "print" command is routed to the scanner and the printer. Simultaneously, channel 2

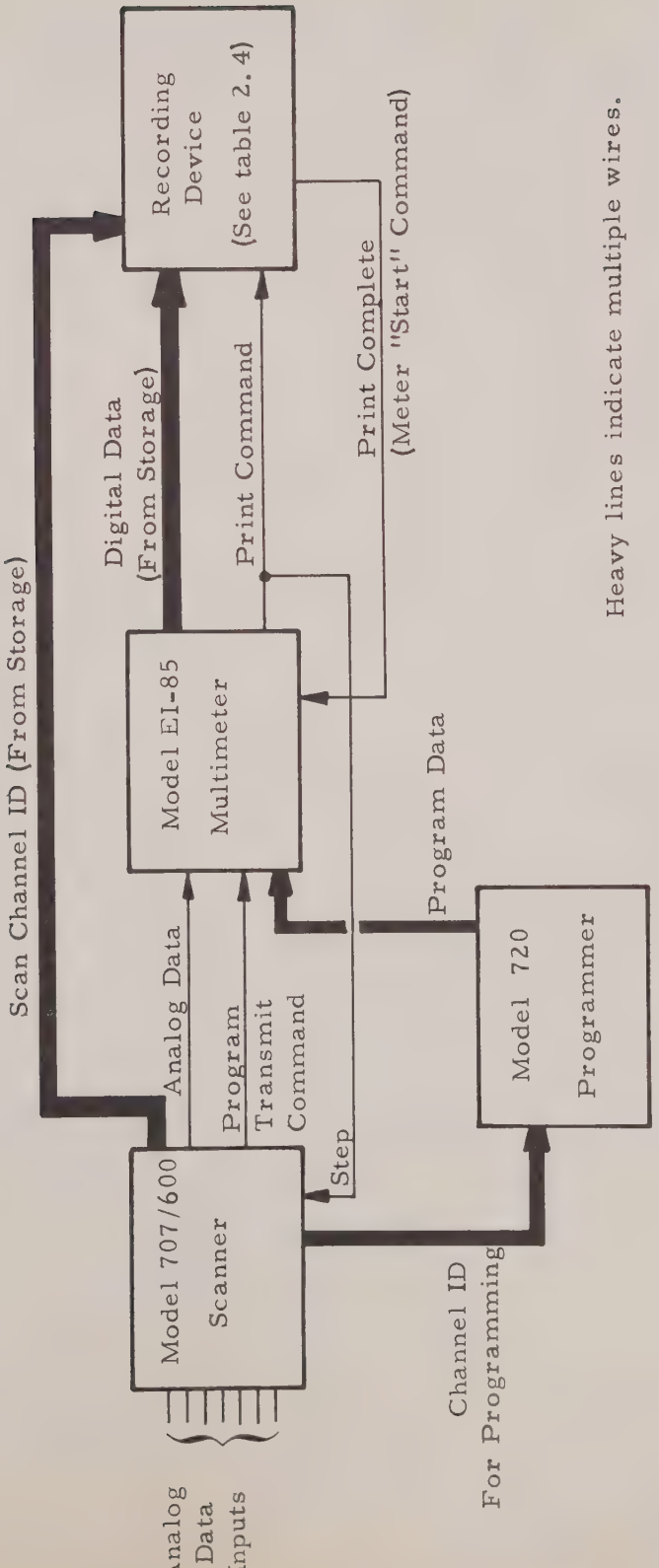


Figure 2.7. Typical System Configuration for Meter "Time Sharing" Operation

is selected by the scanner, the programmer selects program 2, and channel 1 is printed. After about a 25 millisecond delay (scanner switching time), the "remote programming" command is generated by the scanner and program 2 is inserted in the meter. Since the programming time for program 2 is longer than the print time for channel 1 (see Figure 2.8), the "print complete" or "encode" command from the printer is retained by the meter until the programming is complete. At that time, the meter automatically begins the encoding cycle. Simultaneously, channel 3 and program 3 are selected, and channel 2 is printed. After 25 milliseconds, the programming for program 3 is begun. Since channel 2 is printed during the programming time for program 3, the "print complete" or "encode" command is retained by the meter until the appropriate time and channel 3 is then encoded. At the end of the encoding for channel 3, channel 3 is printed and channel 4 is encoded. Thus, the cycle repeats itself with maximum use of available time.

2.11 ALTERNATE METHODS OF OPERATION

Pre-programming operation, is provided by jumper changes as outlined below.

2.11.1 Pre-Programming Jumper

In normal operation, the meter operates in the single encoding mode, however by removing the pre-programming jumper from the outside power supply and control logic board (Figure 2.9), the meter can operate in the pre-programming mode. Single encoding and pre-programming are described in paragraphs 2.10.1 and 2.10.2.

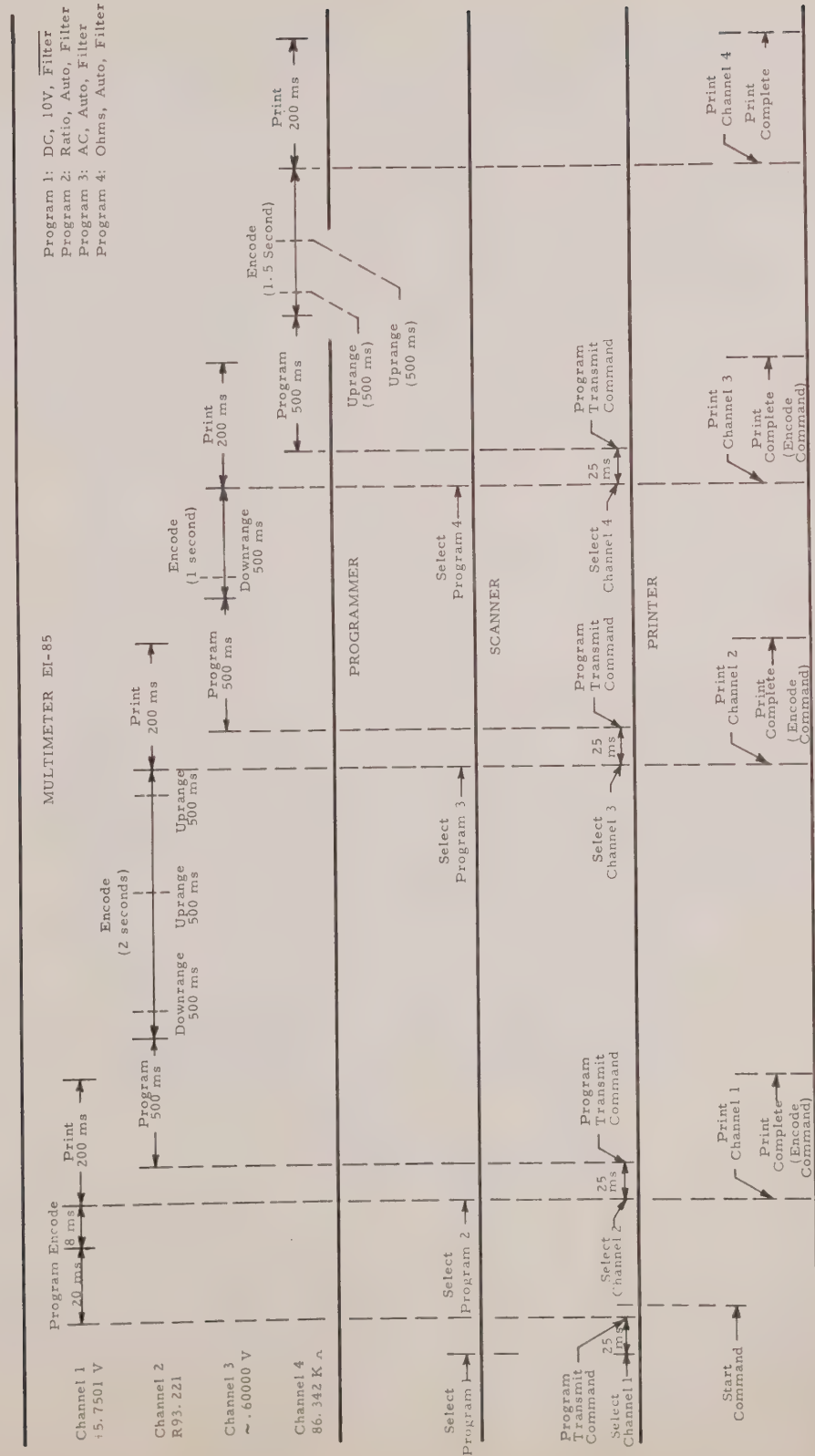


Figure 2.8. Time Distribution in System Operation (Preprogramming Mode)

Table 2.4. Output Recording Devices and Recording Times

Recording Device	Recording Speed (Characters/Sec)	Recording Time (11 Character Word)	Meter Output	Use with HI Output Control
HI Model 9057 (Digital Printer)	---	200 msec	Decimal	---
Tally 420 PR (Paper Tape Punch)	60	180 msec	8421 BCD	Model 825A
Teletype BRPE 110 (Paper Tape Punch)	110	100 msec	8421 BCD	Model 825B
Friden Model 2 (Paper Tape Punch)	20	550 msec	8421 BCD	Model 825C
Friden Flexo-writer (Elec. Typewriter)	9	≈1.2 sec	8421 BCD	Model 825D
Incremental Recorder (Magnetic Tape)	300	≈35 msec	8421 BCD	Model 825E
IBM 526 (Card Punch)	16	1 sec*	8421 BCD	Model 825F
Dura Mach 10 (Electric Typewriter)	15	825	8421 BCD	Model 825G

*Includes delay for card escape and stacking.

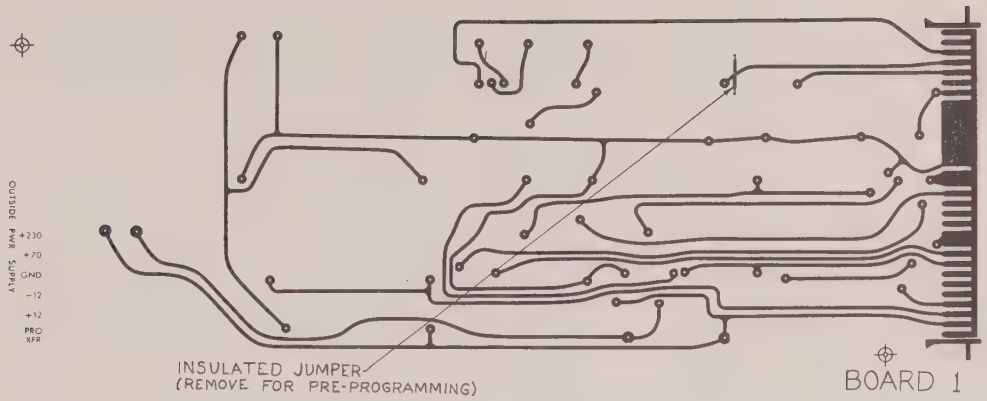


Figure 2.9. Preprogramming Jumper (Outside Power Supply and Control Logic Board)

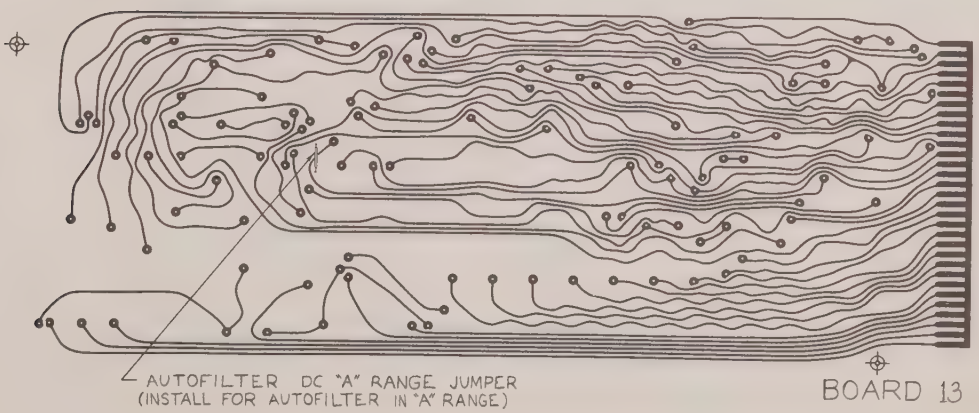


Figure 2.10. Autofilter DC A Range Jumper (Range and Function Board)

SECTION III

THEORY OF OPERATION

3.1 CIRCUIT SYMBOLOGY AND NOTATION

The instrument contains two types of circuits: analog and digital (or logic). Analog circuits are described qualitatively as to how they contribute to the overall operation of the meter. Special circuits are described in detail. A complete manual, in the form of an appendix, is included at the rear of this text to describe the GPA-1 General Purpose Amplifier. Three GPA-1 amplifiers are used in the meter. Digital circuits are described in this manual using standard Boolean Algebra notation, truth tables, logic symbols, and logic (step function) timing charts. A Logic Circuits Symbology-Definitions manual is included at the rear of the text to describe basic logic symbols, equivalent circuits, and theory. Also at the rear of the text is a complete set of logic and/or schematic diagrams for the boards used in the instrument.

3.2 DEFINITIONS

Following is a brief glossary of terms used in this manual to aid in understanding the theory of operation.

Read Cycle: The meter operations from start to finish of any single measurement, including programming and encoding.

Program: The selection of mode, range and filter and the logic signal equivalents. For example, if DC mode, B range and filter are selected, the program would be $\overline{F}_1\ \overline{F}_2$, $\overline{R}_1\ \overline{R}_2\ R_3$ and filter.

Programming: The action of establishing the program in the guarded program logic circuitry, and the associated relay closures and time delays (if applicable). Programming conditions the meter to measure the input signal in the manner prescribed by the program selections. For example, if the input signal is AC, the meter must be programmed for AC; otherwise the meter will perform the measurement prescribed by the mode selection from the previous read cycle. During remote operation, it is possible to set up an incompatible program, such as .1V range in AC mode. The meter has a built-in correction logic that will automatically select a compatible range. In remote operation, selecting a program alone does not complete the programming operation. A start or program command must also be initiated. The selection of the program takes place in the unguarded section of the meter, however the actual program control operations occur in the guarded section.

NOTE

If the program has not changed from the previous read cycle, there will be essentially no programming delay time before the start of the encoding.

Encoding: The process through which the meter determines the magnitude of the signal, registers this value, and delivers that information to the meter readout and electrical outputs. During the encode time, the measurement sequence is performed.

Sequence: The series of operations that take place in the guarded section of the meter after programming is complete and a hold signal is removed from the sequencer. A sequence consists of 36 steps. These steps, and the respective time intervals during which the respective meter operations are taking place, are referred to as S-1, S-2, S-3, etc.

3.3 PRINCIPLE OF OPERATION - GENERAL

Refer to Figure 3.1. The instrument uses a null balance potentiometer to compare the unknown input signal with an internal reference voltage. A precision internal comparison voltage is brought to an exact null balance with the unknown input signal voltage.

The major circuit elements required to encode the unknown signal voltage are:

1. Signal conditioning circuits that scale the unknown input signal voltage to ±10 volts full scale (referred to the output of the input buffer amplifier) and produce a stable, noise-free DC input signal.
2. An internal reference voltage with accuracy and stability of better than 50 ppm (parts per million).
3. A potentiometer that can be controlled by the digital register to produce a feedback voltage containing $(10^5 - 1)$ discrete steps.

4. A comparator to detect differences between the input signal and the feedback voltage of less than 5 ppm.

5. Output circuits to store the digital information between encodings and provide decoding for both electrical and visual outputs.

6. Programming and control circuits to adjust the feedback voltage in a prescribed sequence.

The read cycle starts when the "program" flip-flop on the program logic board is reset. Before a read cycle commences, all circuits remain in the state resulting from the previous encoding, with the exception of the clock which operates continuously. The registers and program logic in both the guarded and unguarded sections contain the measurement magnitude and range information in binary form from the previous encoding while the readout displays that measurement. The input analog signal is conditioned by the input signal conditioning circuitry and directed to the null detector. The null detector compares the input analog signal (E_x) and a feedback voltage (E_{fb}) derived from the precision reference voltage source. The feedback voltage is controlled by the digital register which (at this time) contains the measurement magnitude from the previous encoding. The output of the null detector is converted to logic levels that indicate whether the comparison voltage is less than or greater than the input signal voltage. The comparison of the null detector is a binary decision, that is $E_{fb} > E_x$ or $E_{fb} < E_x$. The fact that a difference exists and the phase of that difference are significant. The magnitude of the difference is not significant. The null detector must detect differences of less than 5 ppm between the two comparison voltages. The $E_{fb} > E_x$ condition is utilized during the encoding process to remove bits from the register as the input signal is being digitized.

The encode sequence consists of a series of 34 clock pulses (S1, S2, S3, etc). Each clock pulse from the sequences is routed through a corresponding gate (G1, G2, G3, etc.), to initiate a logical event in the meter in a prescribed sequence. The 8 clock pulses S1 through S8 are utilized as follows: (1) hi-lo interrogation, (2) down range, (3) polarity, and (4) up range. The 21 clock pulses S9 through S30 are the 22 successive approximation trials, starting with the most significant binary-coded-decimal bit on the highest decade. The guarded register consists of five decade stages corresponding to the five digits in the readout: 10^4 through 10^0. The 10^4 decade is set up in a 2*2221 code; the four lower decades are in 2*421 code. The first measurement sequence clock pulse sets the 2* in the most significant decade (10^4), and in time sequence each bit in the register is

inserted. If an $E_{fb} > E_x$ signal is provided by the null detector, signifying that the comparison voltage is larger than the input signal, the bit is removed. If $E_{fb} < E_x$ is indicated by the absence of an $E_{fb} > E_x$ signal, the bit is allowed to remain in the register. At the end of 21 decisions, 5 for the most significant decade, and 4 for each lower order decade, the bits that remain in the register provide a binary-coded-decimal representation that is equivalent to the value of the measurement magnitude.

At the end of the measurement sequence, the next four sequencer steps reset the unguarded register, transmit the new information to the unguarded register, generate a print command, and set an internal "hold" flip-flop preventing the sequencer from immediately repeating another sequence without first receiving the required start command for the next cycle. The total time required for the series of successive approximation trials, including the control functions, is approximately 7 milliseconds. The binary coded information in the unguarded register is decoded and routed to the readout in 10-line decimal form. Both the binary coded decimal and the 10-line decimal information are made available through the rear panel connectors.

In general, the meter uses negative true logic except in the unguarded register which uses positive true logic. However, both types of logic are contained in either section and changes in the type of logic are called out in the text and in the logic and waveform diagrams.

3.4 UNGUARDED PROGRAM AND CONTROL LOGIC

The unguarded program and control logic is illustrated in Figure 3.2. Before an encoding can commence, the program must be selected either by the front panel ENCODE switch or by remote commands. When the meter is operated by the front panel controls, encodings are initiated individually by single encode commands each time the ENCODE switch is set to the SINGLE (spring loaded) position, or encodings are continuously initiated after the end of each measurement cycle when the ENCODE switch is set to CONT or VAR. When the meter is operated remotely, two methods of remote operation are possible: single encoding or pre-programming. A single encoding is initiated by an AC coupled positive going edge. For pre-programming operation, a jumper wire on the outside power supply and control logic board must first be removed. Pre-programming is then accomplished by the use of two remote signals: a remote program command and a remote encode command. When the program is entered into the meter it is held in the gating at the guard crossing until receipt of the remote program command. The remote program command transfers the program across the guard.

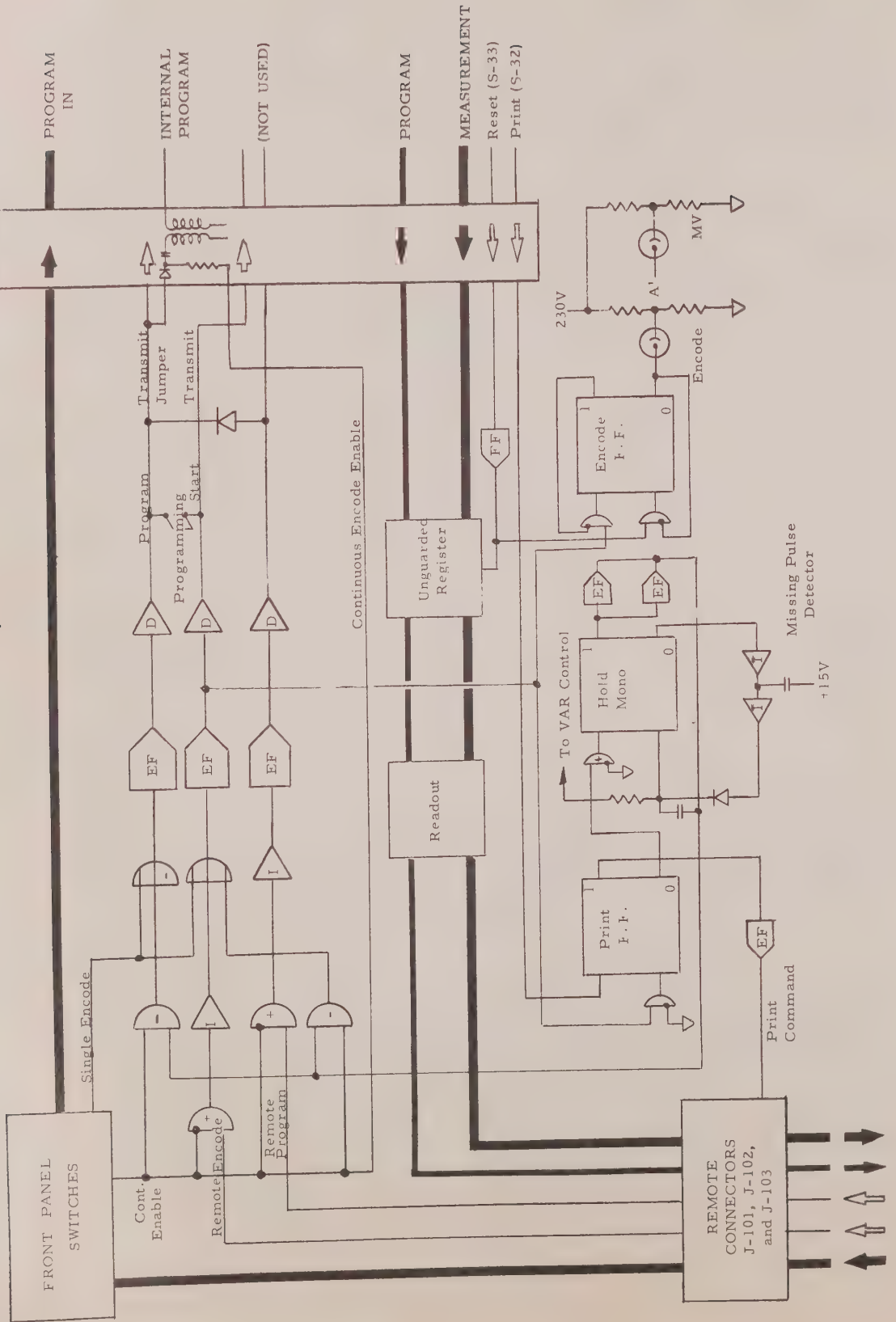


Figure 3.2. Unguarded Program and Control Logic

Table 3.1. Program Logic and Word Designations

MODE	DC	RATIO	AC	OHMS
LOGIC	$\overline{F_1}\,\overline{F_2}$	$F_1\,\overline{F_2}$	$\overline{F_1}\,F_2$	$F_1 F_2$

RANGE (Decimal Position)	A'	A	B	C	D	E
Logic	$\overline{R_1} R_2 R_3$	$R_1 R_2 R_3$	$\overline{R_1}\,\overline{R_2} R_3$	$R_1 R_2 \overline{R_3}$	$\overline{R_1} R_2 \overline{R_3}$	$R_1 \overline{R_2}\,\overline{R_3}$

RANGE (Programming)	MANUAL	AUTOMATIC
Logic	Man	$\overline{\text{Man}}$

Decimal Position (Except A' Range)

A B C D E
↓ X ↓ X ↓ X ↓ X ↓ X

POLARITY	+	-
LOGIC	S	$\overline{S}$

Decimal Position (A' Range)

A'
↓
MV XX ! XXX

* FILTER	IN	OUT
LOGIC	Filter	$\overline{\text{Filter}}$

* The filter is selected automatically in AC, Ohms, A' Range (DC) and A Range (DC)

3.4.1.2 Continuous Encodings

When the ENCODE switch is set to the CONT position, a -15 volts enable level is routed to the control logic circuitry (board 1, pin S) and applied to the enable leg of two ENABLE gates. A second leg on each of the gates is enabled when the external hold mono is false, or at the end of an external hold mono pulse.

The first encoding is initiated by the missing pulse detector (see paragraph 3.4.1.3) which triggers the external hold mono, transistors Q15 and Q16. Q15 is turned on and Q16 is turned off. The level at the collector of Q15 (approximately 0 volts) is routed through a double emitter follower, Q18 and Q19, to the two ENABLE gates. The gates are not satisfied and the program transmit and start transmit lines change from +15 volts to -15 volts.

When the external hold mono returns to its quiescent state (after a pulse duration of approximately .25 seconds) the negative voltage at the collector of Q15 is routed through the double emitter follower and satisfies the two ENABLE gates. The negative going edge thus produced is routed through the program control circuitry and the start program and start transmit commands are generated as described in paragraph 3.4.1.1.

After the first encoding, following encodings are initiated automatically. At the end of each measurement cycle the leading (negative going) edge of the $\overline{\text{print}}$ command triggers the external hold mono and a new encoding is initiated.

3.4.1.3 Variable Encodings

When the ENCODE switch is set to the VAR position the meter operates in a manner similar to that described above except that the external mono pulse duration can be extended from approximately .25 seconds to about 3 seconds by means of the VAR SCALE control. In effect, this reduces the encoding rate.

3.4.1.4 Missing Pulse Detector

In the event that a momentary power failure prevents the program information from crossing the guard, a missing pulse detector circuit generates a transmit command after approximately 15 seconds. The missing pulse detector circuit, Q14, is turned on and off in conjunction with the external hold mono. When the external hold mono is in its quiescent state, Q14 is cut-off, and capacitor C22 charges. When C22 charges to a value great enough to cause Q17 to turn on, the mono is fired again and a new transmit signal is generated.

The missing pulse detector circuit is operational in the continuous and variable operating modes only. It does not affect normal operation, since the normal encoding rate is rapid and C22 charges and discharges with each external hold mono pulse.

3.4.2 Remote Programming

For remote operation, all front panel switches are set in the REMOTE positions. The -15 volts at the arms of the RANGE, MODE, and FILTER switches is routed to remote programming lines at the rear panel connector J-103. Duplicate lines for each switch position are also brought out at connector J-103 and remote programming is accomplished by external form A contact closures, from the remote lines to the desired program considerations (see Table 2.3). In effect, this simulates the front panel switching.

3.4.2.1 Single Encoding

Remote single encoding is initiated by an AC coupled positive going edge from pin z to DD, connector J-103. The positive going edge is brought in pin b of board 1 and AC coupled through an inverter. Operation is then the same as for front panel single encoding.

3.4.2.2 Pre-programming

After the program is entered into the unguarded section of the meter (at the guard crossing gating circuitry), the remote program command (positive going edge) is brought in pin 25 of board 1 to the base of Q8. The signal is inverted, routed through an emitter follower and then inverted again, so that a positive going edge is developed. The positive going edge is then directed through a diode to the program transmit line (see Figure 3.2). The program is transferred across the guard to the guarded program logic. Note that no signal is present on the start transmit line since the pre-programming jumper is removed in this mode of operation. Also there is no signal present on the internal program line, since in the remote mode the continuous encode enable line is positive.

If the program has changed from the previous read cycle, there will be a programming delay during which the sequencer will be inhibited. The sequencer will remain inhibited even after the end of the programming delay, until receipt of the start command. If the start command is received during this delay, it will be retained in storage until the appropriate time for the start of the sequence.

The remote encode command (positive going edge) is brought in pin 24 of board 1 and AC coupled to transistor Q11. The signal is then inverted, routed through an emitter follower and inverted again so that a positive going edge is developed on the start transmit line. This is routed to the reset side of the program flip-flop, resetting it, and allowing the sequence to begin.

3.4.2.3 Guard Crossing

After the program has been entered into the gating at the guard crossing, the entire program crosses the guard in parallel upon receipt of a program transmit command. The unguarded to guarded section guard crossing (board 5) contains 12 program lines. The program lines are coded by letter designations corresponding to program flip-flops in the guarded section (see Table 3.1). Program lines are paired in groups of two, one true and one false for each program consideration. One of each pair must be active or (true) in order to program the meter. However, in the automatic mode, the absence of a signal on the range lines provides for automatic ranging. Six active lines are required at the guard circuitry for the program in manual range, 3 in automatic range.

Program considerations in the unguarded section are in negative true logic. Previous to the program transmit command, the program transmit line is positive. When the program transmit line becomes negative, all true inputs to the program gating charge the respective series capacitors. When the program transmit line becomes positive again, the capacitors discharge and the program information is transferred across the guard to the internal program logic circuits by inductive coupling. In crossing the guard, program considerations are in the form of positive going pulses which are compatible with the PNP type transistors used in the guarded program logic. Refer to paragraph 3.8 for a description of the guarded program logic circuitry.

3.5 SIGNAL CONDITIONING CIRCUITRY

3.5.1 Input Function and Range Switching

Refer to Figure 3.3, a simplified schematic of the input function and range switching circuitry. All relays are de-energized and the signal input is open when power is removed from the meter.

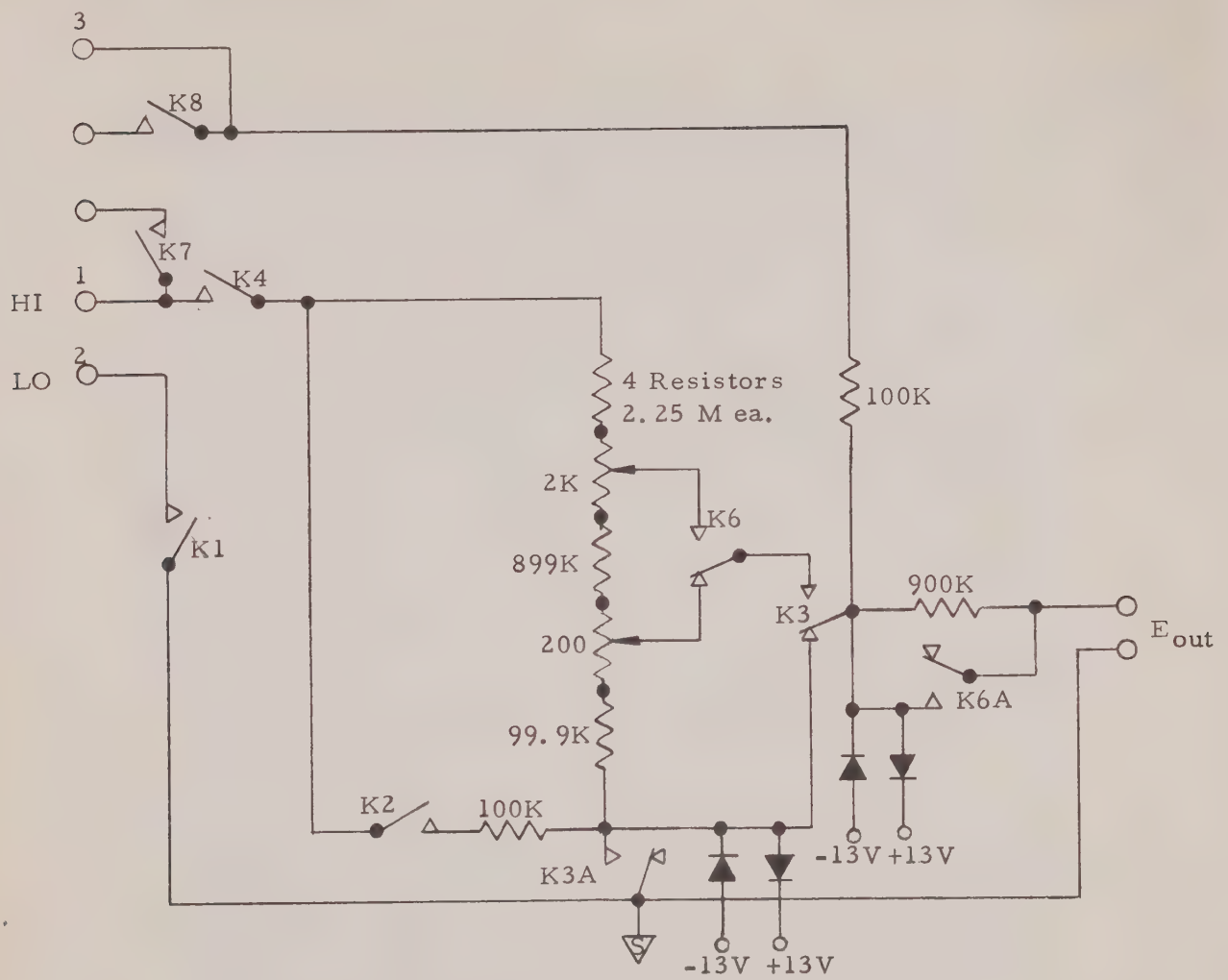


Figure 3.3. Input Function and Range Switching

The function of the input switching circuitry is to switch the input signal leads to either the DC attenuator or to one or more of the accessory options included in the instrument, depending upon the mode of measurement.

The high side of the input signal enters board 15 at P2-1; the low side enters at P2-2. In the lower ranges, signals less than 10 volts, there is no attenuation and the DC input signal voltages are routed directly to the input buffer amplifier on board 16. In the DC and ratio modes of operation, relays K1 and K4 are energized. Relays K2, K3 and K6 switch in appropriate attenuator resistors for higher voltage ranges (see Table 3.2). The output impedance of the attenuator is normalized to one megohm for all ranges of 10 volts and above and normalized to 100 kilohms for all ranges of less than 1.0 volt. The output voltage of the attenuator section is limited by clamping diodes connected to the ±13 volt power supplies.

NOTE

The range setting before the start of an encoding is determined by the last range entered internally by the previous encoding, and is independent of front panel or remote range selection. When the meter is programmed for auto-range, the correct range is switched in during the encoding at S-4 through S-8, or S-14.

In the AC mode, relays K1, K7 and K8 are energized. The input signal is routed through K7 to the AC converter board 19 (refer to AC converter schematic diagram and see section 3.5.3). After attenuation and conversion to DC, the analog DC signal E_{in} is then connected to the input buffer amplifier board 16 through relay K8.

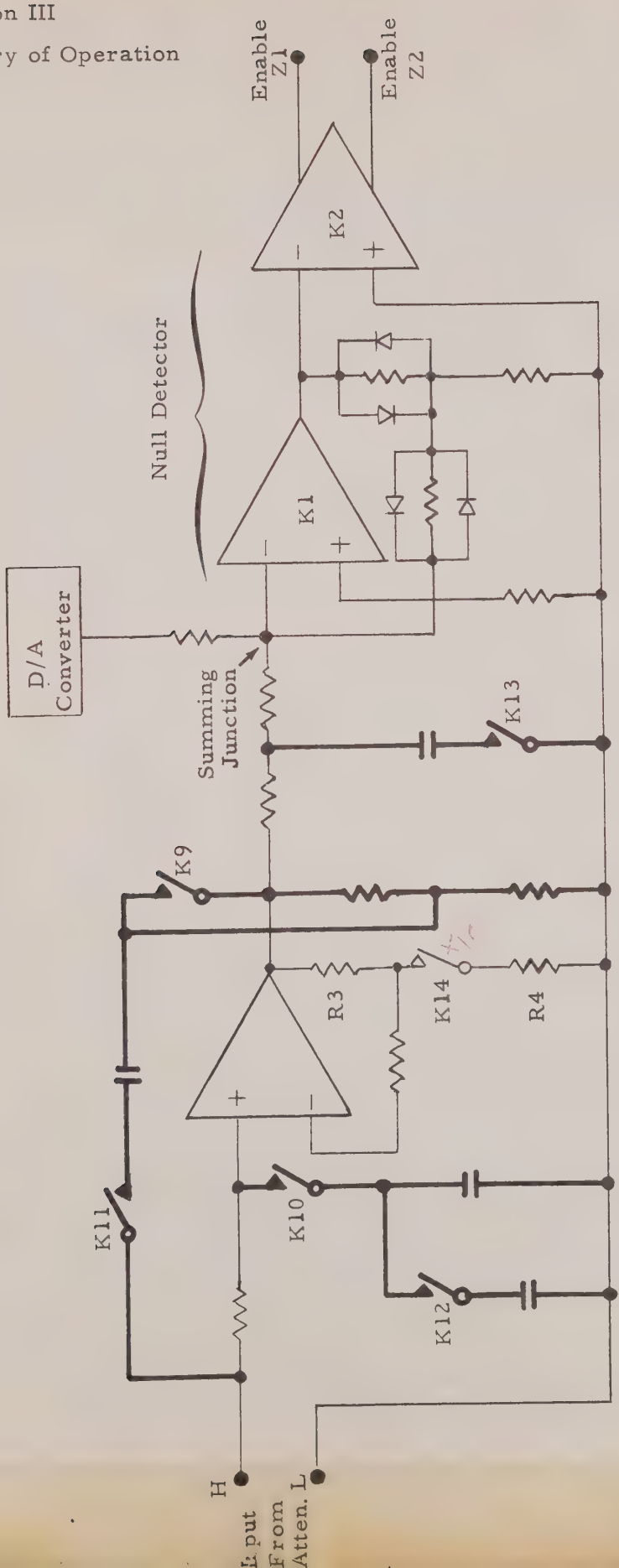
In the ohms mode, the OHMS and REF input terminals are tied together; similarly the HI and LO terminals are tied together. The unknown resistance (R_x) is connected between the two junctions. All relays are de-energized in the ohms mode. The output of the ohms amplifier is brought into board 15 at P2-3 and routed directly to the input of the buffer amplifier on board 16.

3.5.2 Input Buffer and Active Filter

The input buffer amplifier and active filter are contained on board 16. A simplified schematic of the input buffer and active filter circuitry are shown in Figure 3.4. All relays are de-energized for all modes except the 1.0 volt DC range and for the filter-in mode of operation.

The measuring circuits of the instrument are isolated from the signal input leads by a precision potentiometric direct-coupled buffer amplifier. The full-time high imput impedance of the instrument is assured by the utilization of this buffer amplifier, characterized by very low zero drift and a theoretically infinite input impedance. The amplifier is completely solid-state, achieving extremely low voltage and current drift without the use of a conventional chopper stabilizing circuit. The GPA-1 is a four-terminal device, allowing it to be used in either a potentiometric or an operational mode. In the input circuit, the GPA-1 operates as a negative feedback potentiometric amplifier.

Refer to the GPA-1 Appendix at the rear of this text for the basic theory of operation of the amplifier.



NOTE: Heavy Lines Illustrate Active Filter.

Figure 3.4. Simplified Diagram, Input Buffer and Null Detector

As illustrated in Figure 3.4, all relays are de-energized for ranges that exceed 1.0 volt full scale and that do not require filter-in mode of operation. The closed-loop gain of the system is defined by:

$$A_{cl} = \frac{A_{ol}}{1 + \beta A_{ol}}$$

Where: $\beta = \frac{R4}{R3 + R4}$ and $A_{ol} >>> 1$ $(A_{ol} > 120db)$

A_{cl} = amplifier closed loop gain
A_{ol} = amplifier open loop gain

Therefore: $A_{cl} = \frac{1}{\beta} = \frac{R3 + R4}{R4} = 1 + \frac{R3}{R4}$

In the X1 gain configuration, K14 is de-energized and the closed loop gain equals X1, since R = . In the X10 gain configuration, K14 is energized and the closed loop gain equals X10, since $A_{cl} = 1 + \frac{R3}{R4} = 1 + \frac{900K}{100K} = X10$.

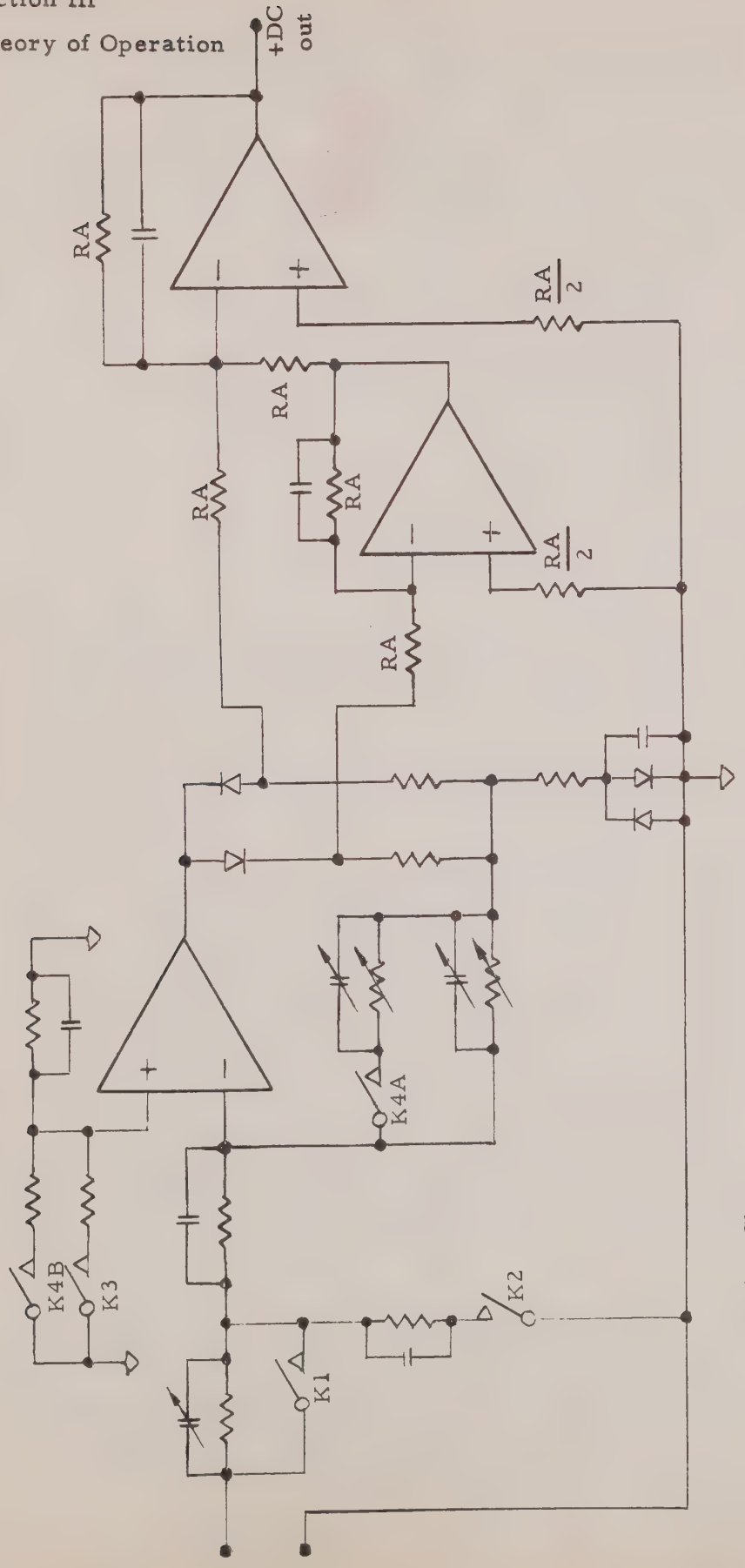
The amplifier is normally operated at X1 gain for all modes and ranges except the 1.0 volt DC range where the gain is switched to X10.

The active filter is illustrated in Figure 3.4 in heavy lines, and can be switched in or out depending upon the programmed mode of operation. The filter is an active three pole Bessel type with the poles chosen to provide an optimum ratio between settling time and noise attenuation. In addition, because of the DC gain switching requirements of the amplifier, it is necessary to switch filter elements. The settling time of the active filter is less than 500 milliseconds to 0.001% of the final value. The normal mode rejection of the filter at 60 cps is in excess of 60 db with a slope of 18 db/octave for higher frequencies.

In the filter mode of operation, relays K10, K11, and K13 are energized. When the pre-amplifier range is selected, relays K9 and K12 are also energized to change the poles of the filter. The gain of the amplifier is switched from X1 to X10 gain by relay K14.

3.5.3 AC Converter

The AC converter is a signal conditioning plug-in circuit card (board 19) to allow AC voltages to be measured with the normal voltmeter input leads. The AC converter uses a precision rectifying circuit to convert the unknown AC voltage directly to DC, and the resulting DC is read to 5-digit resolution by the DC measuring circuits.



Relay Chart

	K1	K2	K3	K4
1V	X			
10V	X			X
100V		X	X	
1000V		X	X	X

Figure 3.5. Simplified Diagram AC Converter

The AC-to-DC converter output voltage corresponds to the average value of the input waveform and scales the output to indicate the RMS value of a sine wave, i.e. $E_{RMS} = 1.11\ E_{AVG}$. Since the converter must present a stable and precise DC output, the active filter is energized during the AC mode of operation.

A simplified block diagram of the converter is shown in Figure 3.5. The attenuator and beta (β) network conditions the amplitude of the voltage to be measured and applies the voltage to the converter amplifier.

The converter amplifier is a precision rectifier with a plus (+) and minus (-) output. The voltage at these outputs is in a half-wave pulsating form and this is not suitable for direct measurement by the DC measuring circuits. The inverting amplifier inverts the plus (+) output voltage and applies it to one input of the post summing amplifier. The minus (-) output voltage is applied to the other input of the post summing amplifier. The output voltage of the post amplifier, in the absence of the 0.1 μf capacitor, would be a full-wave rectified DC voltage. The capacitor serves to filter the output voltage to the desired degree. Since the signal to be filtered is full-wave rectified, as opposed to half-wave rectified, a smaller capacitor can be used for the same ripple magnitude in the output. The smaller time constant results in a faster response time for the converter.

The inaccuracies caused by the output diode drops in the precision rectifier are eliminated as a source of non-linear error by the large forward gain of the amplifier. The long term stability of the AC-to-DC converter is assured by the use of precision resistors in the input attenuator and in circuit areas which determine amplifier gain stability.

3.5.4 Pre-Amplifier and Ohms Amplifier

A simplified diagram of the pre-amplifier and ohms amplifier is shown in Figure 3.6. The pre-amplifier and ohms amplifier allows the instrument to resolve DC voltage to one microvolt with the normal voltmeter input leads and to measure resistance with a modified lead configuration. The printed circuit card includes three plug-in assemblies: (1) a standard GPA-1 amplifier (refer to Appendix No. 1) and (3) a drift compensation circuit. The function of the circuit is controlled by appropriate relay closures as command by the range logic and the mode selection. The GPA-1 operates as a negative feedback potentiometric gain of one hundred (X100) amplifier in the preamplifier mode of operation and as an operational amplifier in the ohms mode of operation.

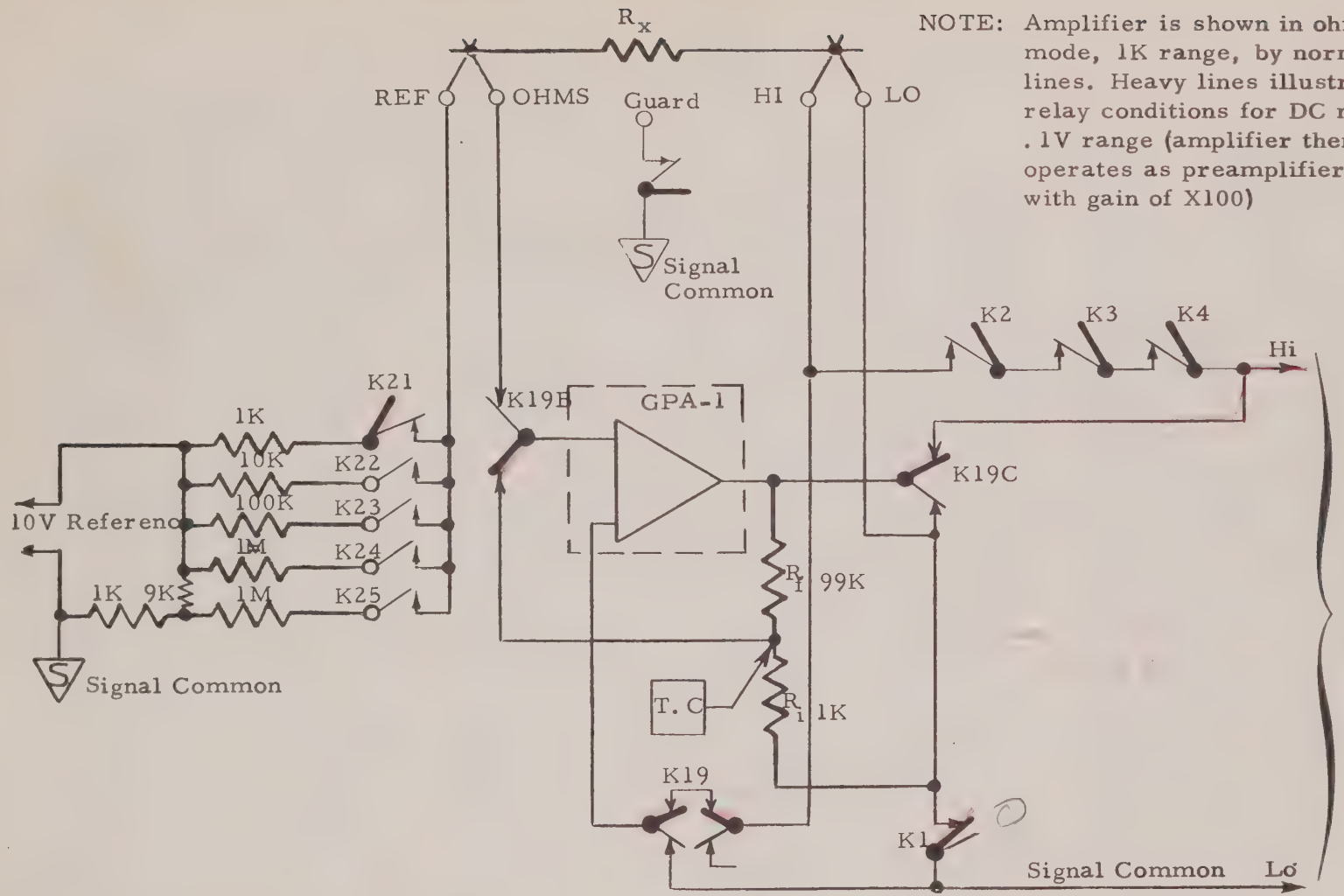


Figure 3.6. Simplified Diagram of Preamplifier and Ohms Amplifier

3.5.4.1 Ohms Converter

Refer to Figure 3.6. The unknown resistances are converted to proportional DC voltages ranging from 0 to 10 volts full scale, utilizing the operational amplifier with a known input current. The test resistance is connected in the operational feedback path of the amplifier to obtain an output voltage that is proportional to the product of the input current and the test resistance. The output voltage of the ohms converter is filtered by the active filter before being applied to the DC measuring circuits. The relationship of the unknown test resistance to the DC output voltage is defined as follows:

$$E_r = -E_{ref} \times R_x / R_{std}$$

Where: E_{ref} equals -10V

R_x is the unknown test resistor

R_{std} is the precision input range resistor selected by the ohms attenuator relays

E_r is an analog voltage directly proportional to the unknown resistance

In order to avoid errors due to test lead resistance when measuring low resistances, a modified four-wire technique is used. This technique is illustrated in Figure 3.7.

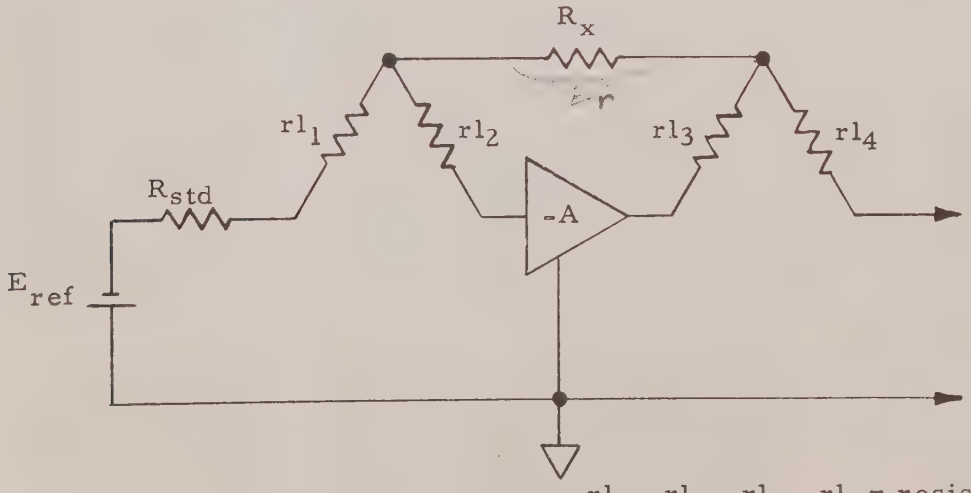


Figure 3.7. Four-Wire Resistance Measurement

The effect of rl_1 is small compared to R_{std}. A trim adjustment in in series with R_{std} allows for compensation of lead resistance. The effect of rl_2 is negligeable because of the amplifier high input impedance. Current through rl_2 approaches zero. The effect of rl_3 is zero, since the output is sensed directly at the output terminal. The effect of rl_4 is zero, since the input impedance of the DC measuring circuits is large (10^9 ohms).

The input cable to the instrument consists of five difference leads and it is important that each lead by connected properly for resistance measurements. The ohmmeter lead functions are listed below:

REF: Delivers current to test resistance (limited to 10 ma maximum at 1 KΩ)

LO: Accept current

OHMS: Senses voltage at low end of test resistance

HI: Senses voltage at high end of test resistance

GUARD: The guard is connected to the floating shield (if any) of the device being measured. The GUARD terminal must not be connected to the unknown resistance or ground as the guard shield is internally grounded.

The function relay K19, located on board 18, is de-energized for the ohms mode and energized for the pre-amplifier mode. The range attenuator relays K21 through K25 inclusive, as controlled by the range logic, determine the input current to the operational amplifier. The input current for the 1KΩ range is 10 ma, and is proportionally reduced to 0.001 milliamps for the 10 megohm range. The calibration adjustments for the five ohmic ranges are also included on the ohms attenuator sub-assembly plug-in circuit board. Table 3.2 lists the current flowing in the test resistance and the power dissipation.

Table 3.2. Current and Power Dissipation in Test Resistance

RANGE	CURRENT	POWER DISSIPATION
1K	10 ma	100 mw
10K	1 ma	10 mw
100K	.1 ma	1 mw
1M	.01 ma	.1 mw
10M	.001 ma	.01 mw

3.5.4.2 Pre-Amplifier

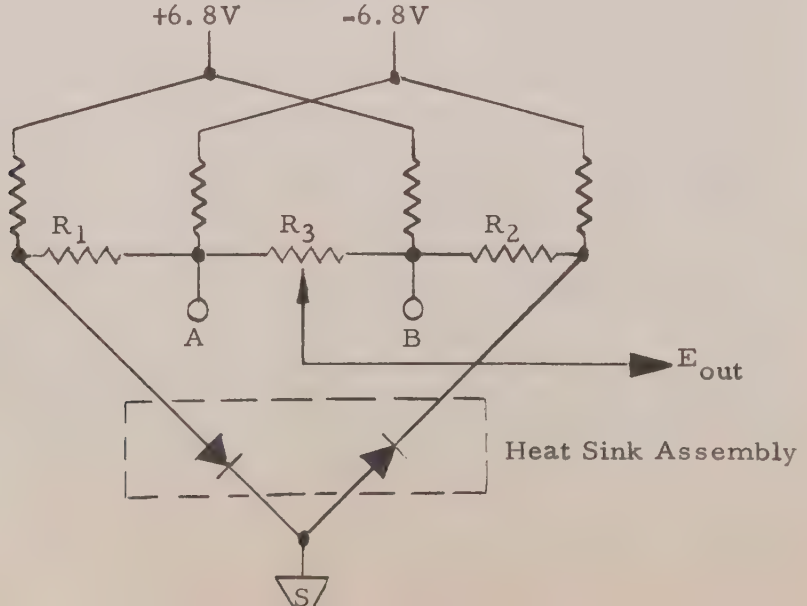
The function relay K19 is energized for the pre-amplifier mode of operation and is controlled by the range logic. The DC input attenuator is bypassed by de-energizing relays K1 and K4 (input function and range board 15), and connecting the output of the pre-amplifier directly to the input buffer amplifier. Note that the active filter is energized and the input buffer is switched to a gain of one (X1). The function relay K19, switches the pre-amplifier GPA-1 so as to connect it in the X100 potentiometric mode of operation. Therefore, by cascading the two amplifiers, the resolution of the instrument is increased to one microvolt or 0.1V full scale.

The pre-amplifier includes a zero adjustment and calibration control that are located for easy access on the front of the plug-in circuit board.

3.5.4.3 Temperature Compensation Circuits

Temperature compensation circuits are used to improve the circuit operation of the precision amplifiers over the operating environment temperature range. Each circuit is basically a bridge with a silicon diode in two of its legs. For the GPA-1 amplifiers, the temperature compensation diodes are on a separate assembly mounted to the heat sink of the input transistor pair of the GPA-1. The diodes are so located as to assure a good thermal bond to the input transistor. The forward drop characteristics of the silicon diodes decrease approximately 2 millivolts per degree centigrade rise. The rate of voltage change per degree temperature change for the temperature compensation circuit is adjustable to compensate a particular amplifier.

A simplified schematic diagram of a temperature compensation bridge for a GPA-1 amplifier is shown in Figure 3.8.



3.6 REFERENCE FEEDBACK CIRCUITRY

The reference feedback circuitry consists of precision reference voltage supply, a buffer amplifier, and a digital potentiometer or digital-to-analog converter.

3.6.1 Precision Reference Supply

The reference supply and buffer amplifier plug-in circuit boards are contained on the reference buffer amplifier board 16. A simplified schematic diagram of the reference and buffer amplifier is shown in Figure 3.9. The reference supply is used to provide a constant reference voltage for all modes of operation except ratiometer. In the ratio mode, the reference voltage is obtained from the external reference source. The output of the buffer amplifier provides the load current to the D/A converter and the ohms attenuator.

The reference supply consists of a zener diode connected in one leg of a bridge and a four-terminal amplifier connected in a negative feedback potentiometric configuration. The amplifier provides isolation to line voltage variation, has a scale factor (K) to adjust output voltage to 10 volts, and maintains a constant current in the zener diode. The non-inverting input of the amplifier is connected to a fixed reference voltage supplied by a zener diode and the inverting input is connected to a resistor feedback network. The resistor feedback network provides gain to the loop, so that $E_Z \times K = 10$ volts. The zener current is supplied by the amplifier through a resistor connected from the output of the amplifier to the zener diode. The temperature compensation bridge assures stability over the temperature range of 5° C to 45° C.

The buffer amplifier not only supplies the current demand of the D/A converter but also provides for polarity reversal of the feedback voltage. The buffer amplifier has two operation modes, operational and potentiometric, which are selected by means of relays K15 through K18. When the meter is measuring a positive voltage, relays K16 and K18 are energized and the amplifier is connected in an operational configuration with a gain of -1. Thus, the +10V precision reference is inverted to -10V. In the negative polarity, relay K15 is energized and the amplifier is connected in a potentiometric configuration with a gain of +1. In this mode, the precision reference voltage is non-inverted and remains +10V.

In the ratio mode, relay K17 is energized and the amplifier is connected in an operational configuration, inverting the external reference voltage. Since the polarity of the external reference voltage and the input signal

voltage are the same for ratio measurements, the buffer amplifier provides the reference inversion required by the measurement technique. The external reference can be any value from 0 to ±10 volts, however, the instrument's resolution is inversely proportional to the reference voltage, i.e. resolution equals $\frac{10}{E_R} \times .001\%$.

Therefore, if the external reference voltage is 5 volts, the resolution of the meter is .002% of full scale or 2 digits.

In the ohms mode, relay K16 and K18 are energized and the amplifier is connected in an operational configuration. The -10 volt output is connected to the ohms attenuator and the D/A converter as the reference voltage. In all modes, the buffer amplifier provides an extremely stable output and presents a low output impedance to the D/A converter bridge current load demands.

3.6.2 Digital to Analog Converter

The D/A converter converts the digital number contained in a binary coded decimal register (see paragraph 3.10) into a proportional discrete analog voltage. The circuit as controlled by the register will produce a feedback voltage containing 99999 discrete steps at a constant output impedance of 40 kilohms. In essence, the D/A converter is a bridge, consisting of 5 groups of resistors. Each group corresponds to a decade and each resistor in a group corresponds to the weight of one bit in the register. All resistors are connected through electronic transistor switches (connected as a single pole double throw switch) to either the precision reference voltage (paragraph 3.6.1) or to signal ground, depending upon the state of the respective flip-flop in the register. When the Flip-Flop is reset, the shunt transistor switch is turned on and the resistor is connected to ground. Conversely when a flip-flop is turned on, connecting the resistor to the precision reference voltage. The voltage at the summing junction reflects the output of the 10^2 decade in volts, the 10^3 decade in tenths of a volt, the 10^4 decade in hundredths of a volt, and so on. The voltage at the top of each attenuator resistor is summed with the voltages from the lower decades and the cumulative voltage at the top of the bridge is the sum of the incremental voltages developed across each decade.

3.7 NULL DETECTOR AND CONTROL LINE CIRCUITRY

3.7.1 Null Detector

See Figure 3.4. The null detector circuitry is contained on board 16 with the input buffer amplifier and active filter. The input analog signal that is conditioned by the input signal conditioning circuitry is

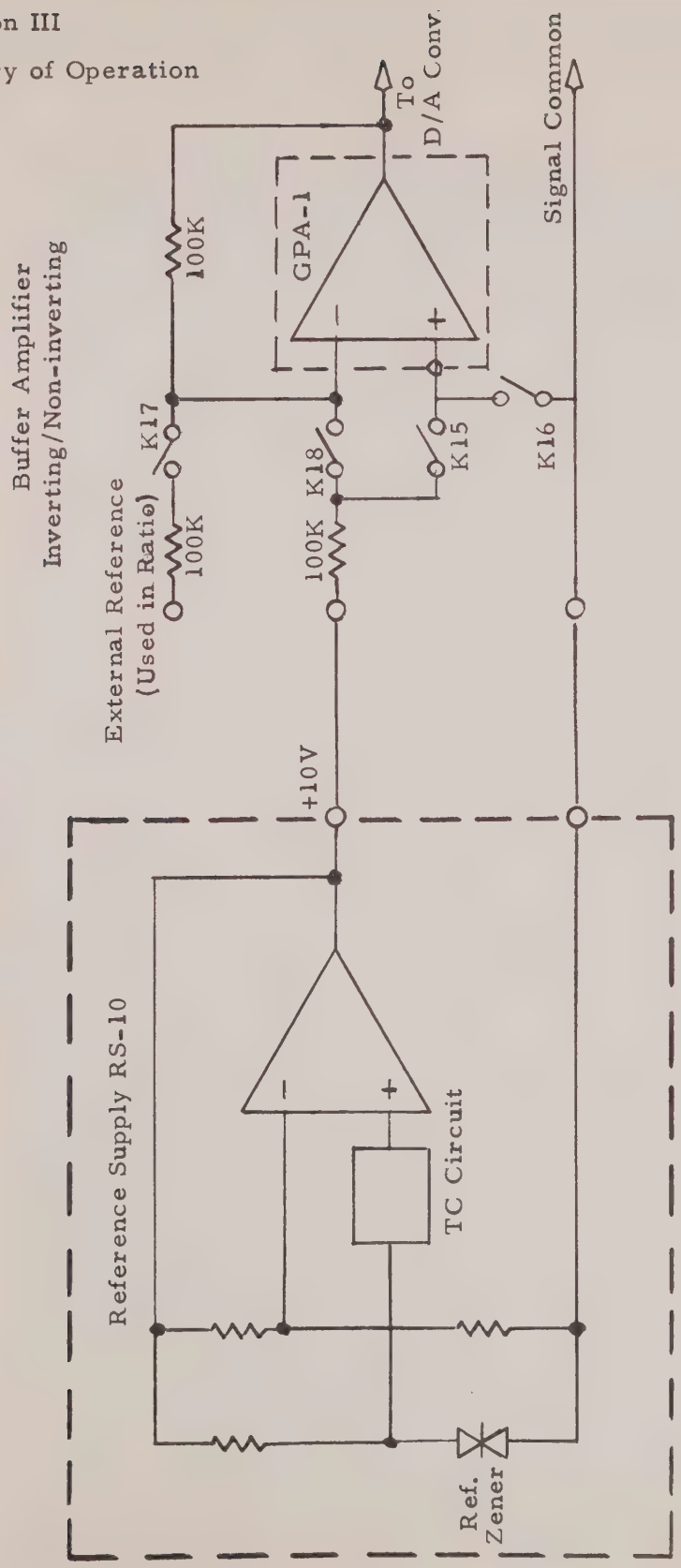


Figure 3.9. Simplified Diagram of Precision Reference Supply and Buffer Amplifier (Inverting/Non-inverting)

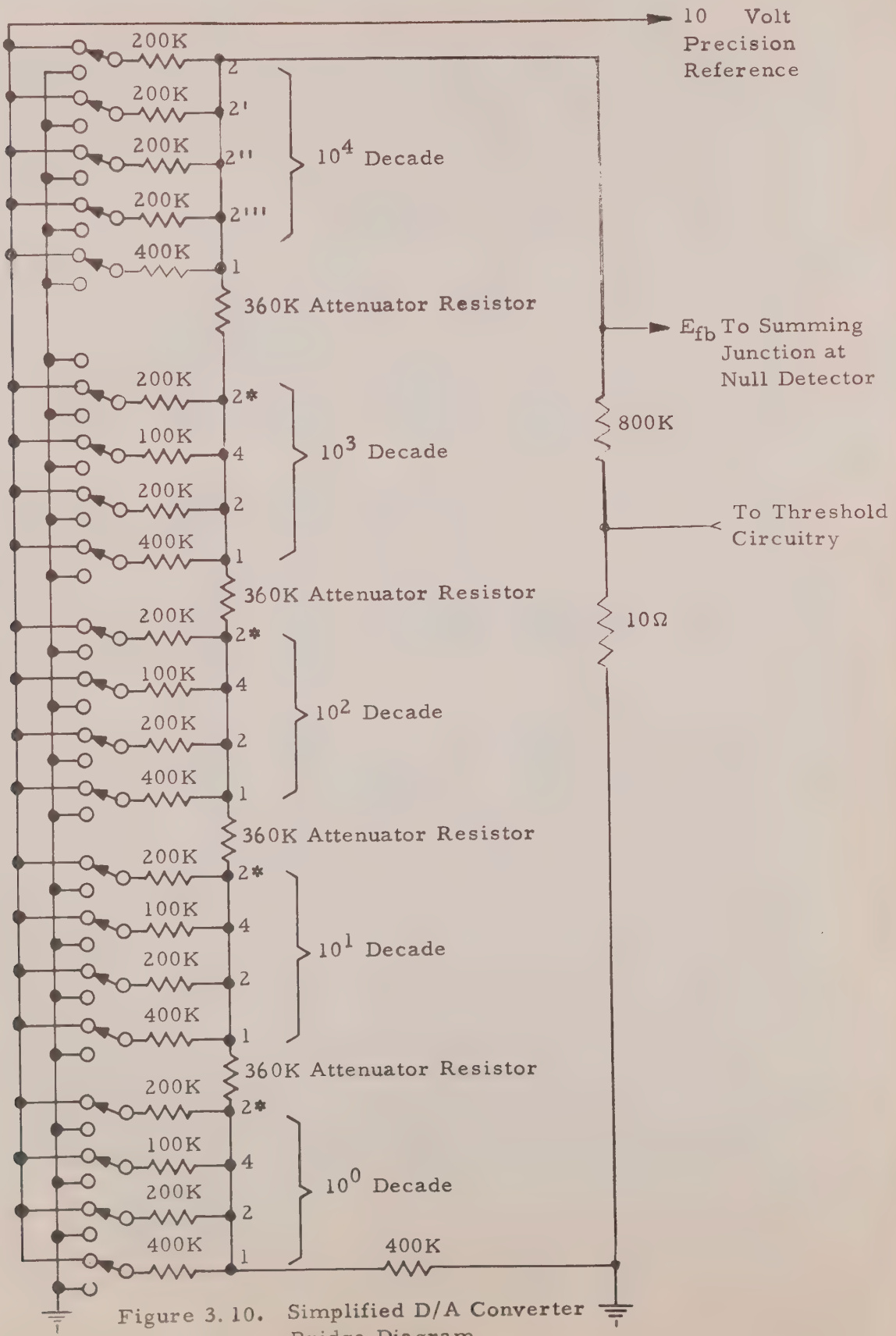


Figure 3.10. Simplified D/A Converter Bridge Diagram

connected through a string of precision resistors and summed with the feedback voltage from the D/A Converter. The summing junction is connected to the input of the null detector. The null detector compares the input analog signal (E_x) and the feedback voltage (E_{fb}) to ascertain whether E_{fb} is less than or greater than E_x. The output of the null detector is converted to logic levels that indicate whether the comparison voltage is less than or greater than the input voltage. The comparison of the null detector is a binary decision, that is $E_{fb} > E_x$ or $E_{fb} < E_x$. The fact that a difference exists and the phase of that difference are significant. The magnitude of the difference is not significant. The polarities of the two voltages E_{fb} and E_x are out of phase. When E_{fb} is positive E_x is negative, and vice versa. The design of the null detector is such that it will detect differences between the two comparison voltages of less than 5 ppm. The $E_{fb} > E_x$ condition is utilized during the encoding process to remove bits from the register as the input signal is being digitized.

The null detector actually consists of two amplifiers, K1 and K2. K1 is connected as an operational amplifier with a closed loop gain of approximately 1000. K2 is a potentiometric amplifier with a gain of approximately 200 and provides an inverted and non-inverted output. The feedback network of amplifier K1 is shunted by diodes to provide non-linear feedback around the amplifier for large input signals. During the encoding process, large differences exist between the two comparison voltages and the non-linear feedback prevents the amplifier to saturate.

The operational amplifier, K1, consists of two differential stages, Q1, Q2, Q4, and Q7. This amplifier provides a single-ended output with very high gain while maintaining the differential amplifier high common mode rejection. The balanced configuration is maintained throughout the circuit providing excellent immunity to power supply coupled drift and noise. The output differential stage is isolated from the input stage by emitter followers Q3 and Q5 to improve the open loop gain characteristics of the input stage. R135, R137, R138, and CR67 through CR70 provide the feedback network for gain determination. Power supply isolation is provided by zener diode CR76 and CR78.

The post amplifier has two differential stages, Q8 through Q11, providing a differential mode output required to drive the logic levels of the digital circuitry. The closed loop gain of the amplifier is controlled by feedback from the output stage collectors to the input stage emitters. The feedback network consists of R162, R163, R159 and R161.

3.7.2 Control Line Circuitry

See Figure 3.11. The control line circuitry is contained on the clock board 11. The null detector outputs, enable Z1 and enable Z2, are gated with the clock to set either the Z1 or Z2 control flip-flop. The Z1 and Z2 flip-flop outputs are gated with the state of the polarity (S) flip-flop, and the gated signal is used as the control line. The gates are satisfied and the control line is true only when an E_{fb} E_x (absolute values) condition exists.

In positive polarity, Z2 and S are gated to generate control line signals. Z2 is set at the coincidence of enable Z2 and clock signals. Z2 is reset by the clock signal.

In negative polarity, Z1 and S are gated to generate control line signals. Z1 is set at the coincidence of enable Z1 and clock signals. Z1 is reset by the clock signal.

3.8 GUARDED PROGRAM AND CONTROL LOGIC

3.8.1 Program Control and Delay

The program control and delay circuitry is contained on the program logic board 12 (see schematic at rear of text). A simplified logic diagram of the program control circuits and sequence delay waveforms is illustrated in Figure 3.12.

At the start of a read cycle the program is transferred across the guard. Then, depending on the nature of the program and the type of encoding, the meter will either start the encoding almost immediately or be delayed until after the programming is complete. Three different programming delays are provided to either allow for relay settling time and/or filter slewing (if necessary), or allow the meter to start the encoding almost immediately (if the program has not changed and filter is not needed). The program modes are discussed below:

a. Filter out mode and no program change

In the event that the program is the same as that from the previous read cycle and the meter is not in a filter mode, the guarded program logic will be unaffected by the transferral of the program across the guard. The start or internal program command from the unguarded section will reset the program flip-flop. The set output from the program flip-flop will go false at this time and initiate a reset command to the delay circuit.

The delay circuit is a special logic device that sets when a positive level is applied to the input, and resets approximately 2 ms

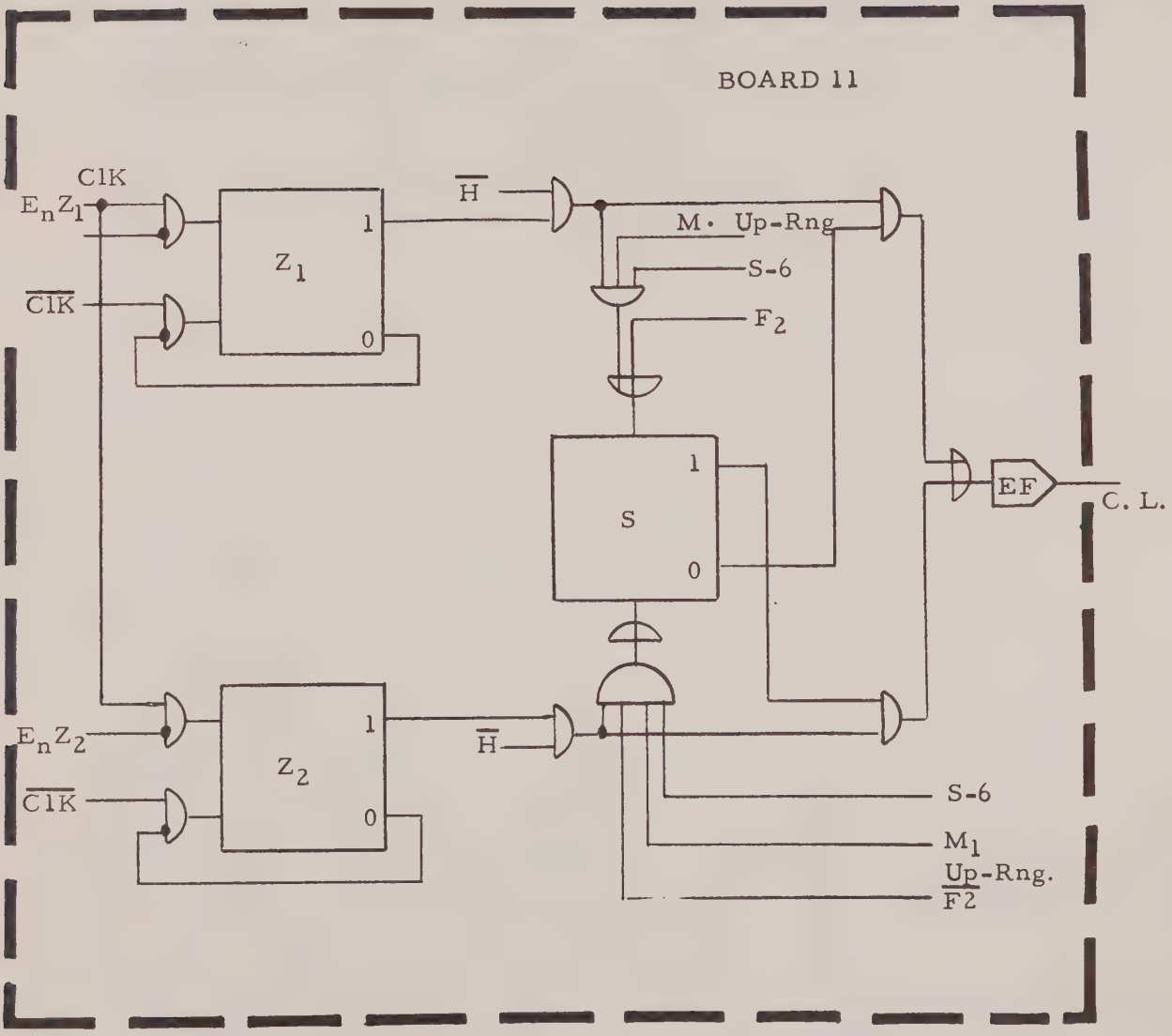


Figure 3.11. Control Line Circuitry

after a negative level is applied to the input. The delay circuit will follow the leading edge of M1, M2, or program, and will lag the trailing edge of the last of these signals to go false. Refer to the OR gate and inverter connected to the input of the delay circuit in Figure 3.12.

The output of the delay circuit is routed through an AND gate and an OR gate to the sequencer hold inverter. The output of the sequencer hold inverter would hold the sequence until the end of the delay time; however the sequence is already held by the H (hold) F.F. which was set at the end of the last encoding.

At the end of the nominal 2 ms delay, the reset state of the delay circuit resets the H bit and releases the sequencer hold. The sequence begins at this time.

b. Filter out mode and program change

A change in program will initiate a change in the state of the range and/or function flip-flops, upon receipt of the program in the guarded section. This change will be sensed by the program change circuitry. The leading edge of the output of the changed bit is routed through an ENABLE gate, an OR gate, and an inverter to the program change line. This trigger signal is gated with the H bit at the input of M1, and M1 is triggered. The duration of the M1 signal is approximately 18 ms in the filter-"out" mode.

During the M1 time, the H bit and delay circuit are set. At the end of M1, an additional 2 ms delay is provided by the delay circuit. Upon termination of the delay signal, the H bit is reset and the sequence will start (if a start or internal program command has been received by this time). In the preprogramming mode of operation there may be a delay before the start command is received. The arriving start command will reset the program flip-flop, enabling the reset AND gate to the H bit, and the sequence will start.

c. Filter in Mode

The filter delay is initiated either by a program change or the start command. If the program has changed, the program change command gated with the H bit will trigger M1. In the filter mode, a capacitor is switched into the circuitry of M1, causing the time duration to be increased to approximately 250 ms. Also, in the mode, M2 will be triggered by the trailing

edge of M1 by means of a positive ENABLE gate followed by an inverter. The time of M2 is approximately 250 ms. The delay circuit will be set by the leading edge of M1 and reset approximately 2 ms after the trailing edge of M2, providing a total time of approximately 500 ms.

If the program has not changed, M1 will be triggered by either the start or internal program command gated with the set output of the filter F. F. M2 and the delay circuit will be triggered as described in the previous paragraph.

The sequence will begin at the end of the delay when the H bit is reset. When the instrument is in the preprogramming mode, the sequence will start when a start or internal program command is received.

3.8.2 Program Logic and Relay Drivers

The program logic flip-flops are contained on boards 11 and 13 (see schematics at the rear of this text). Flip-flops F1 and F2 (mode) are contained on the clock board 11. Flip-flops R1, R2, and R3 (range) and the filter flip-flop are contained on the range, logic board 13. The manual range (man) flip-flop is contained on board 11. Figure 3.12 illustrated the man flip-flop and Figure 3.13 illustrates the mode flip-flops, range flip-flops and filter flip-flop.

After crossing the guard, the program is directly routed to the program flip-flops. The outputs of these flip-flops are gated according to the program logic (Table 3.1) and routed through relay drivers on board 13 to the corresponding range and function relays on boards 16, 17, 18 and 19 (refer to Table 3.3 for the relay chart). The set outputs of the program flip-flops are also routed to the guard gating so that at the end of the encoding the program information can be transferred back to the unguarded section. In manual ranging the man flip-flop is set by either the set R1 or reset R1 program command. The sequencer lock flip-flop (see Figure 3.12) is set only during automatic ranging. If the man flip-flop is set, the sequencer lock flip-flop remains in its reset state during the ranging portion of the sequence, and no range up-count pulses will occur.

3.8.3 Sequence Delay Logic and Associated Circuits

The sequence of operation in the guarded sections of the meter may be stopped or delayed at various times by four logic levels generated on the program logic board 12 and the power supply and hi-lo board 7: the hold bit (from the hold flip-flop, board 12), the sequencer hold

If the program is the same as for the previous read cycle, the guarded program logic will remain unchanged. If the program has changed, the appropriate program flip-flops will register this change, a program change command will be generated, and a delay will be initiated, during which time the program relays will settle and the encoding will be inhibited. The remote encode command can be received before or after the end of the program settling time and will be retained until the appropriate time for the start of the sequence.

At the end of an encoding the program is transferred back across the guard and entered into the unguarded register, and a print command is generated. The unguarded register controls the readout and electrical outputs.

3.4.1 Front Panel Switching

Refer to the front panel switches and logic schematic diagram. The arms of all front panel switches are connected to -15 volts. When the arms of the RANGE, MODE and FILTER switches make contact with selected positions, -15 volt (true) signals are routed to corresponding coded lines and then to the gating at the guard crossing assembly; the program gates are inhibited until receipt of a program transmit command. Program code designations on the coded lines correspond to program logic in the guarded section of the meter (see Table 3.1).

3.4.1.1 Single Encoding

When the ENCODE switch is set to the SINGLE (stationary) position, a -15 volts enable level is removed from the control logic circuitry. If the ENCODE switch is then set to the SINGLE (spring loaded) position, a negative pulse is brought in pin b of the outside power supply and control logic board 1. This pulse is directed through two separate OR gates (diodes CR25 and CR18) to the input of emitter followers Q13 and Q10. Duplicate signals are then routed to drivers Q12 and Q9, and two simultaneous pulses - a program transmit and a start transmit command - are generated. Both pulses are positive going, from -15 volts to +15 volts.

The program transmit command enables the program gating at the guard crossing, and the program, which was inhibited until this time, now crosses the guard to the guarded program logic. The start transmit command crosses the guard and resets an internal program flip-flop. This allows for the start of the sequence at the end of the programming operations.

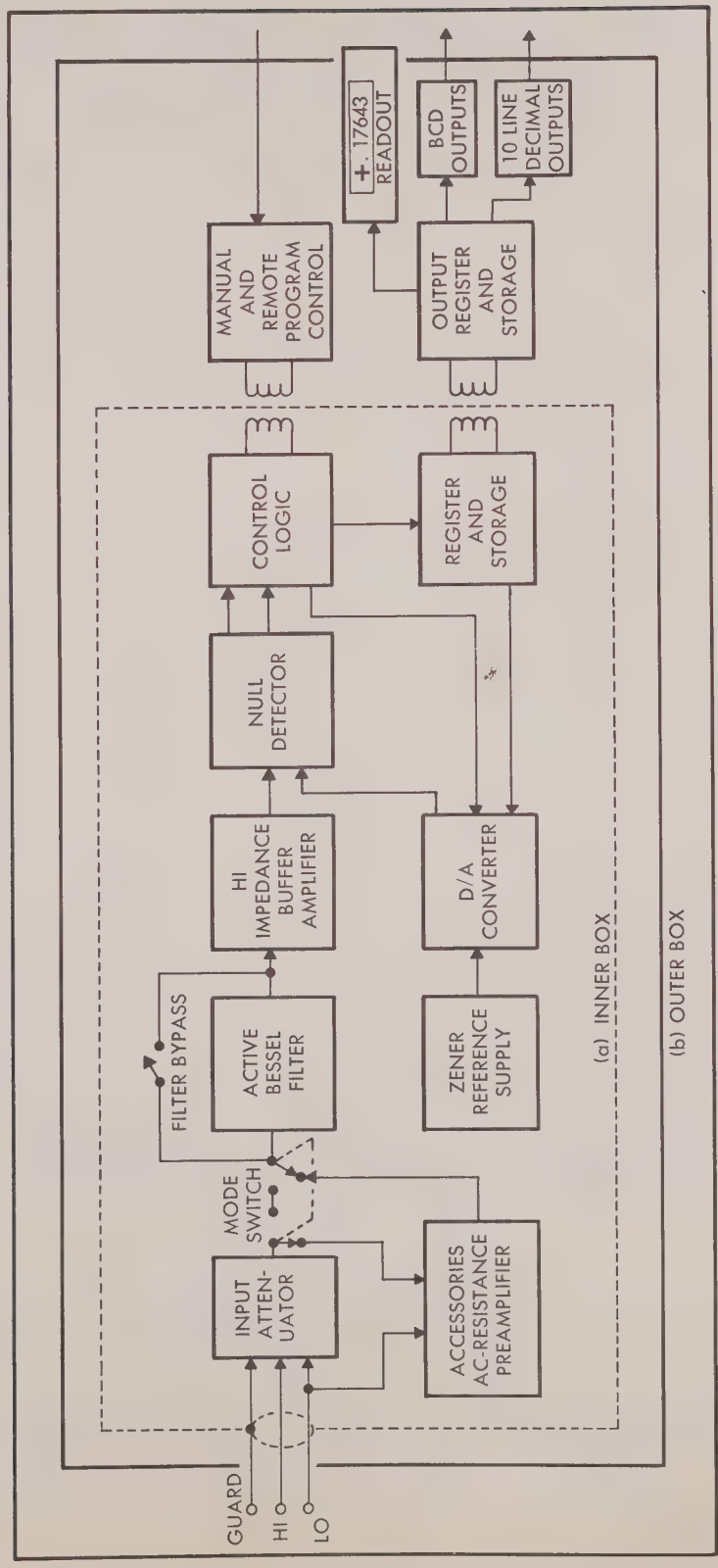


Figure 3.1. Block Diagram

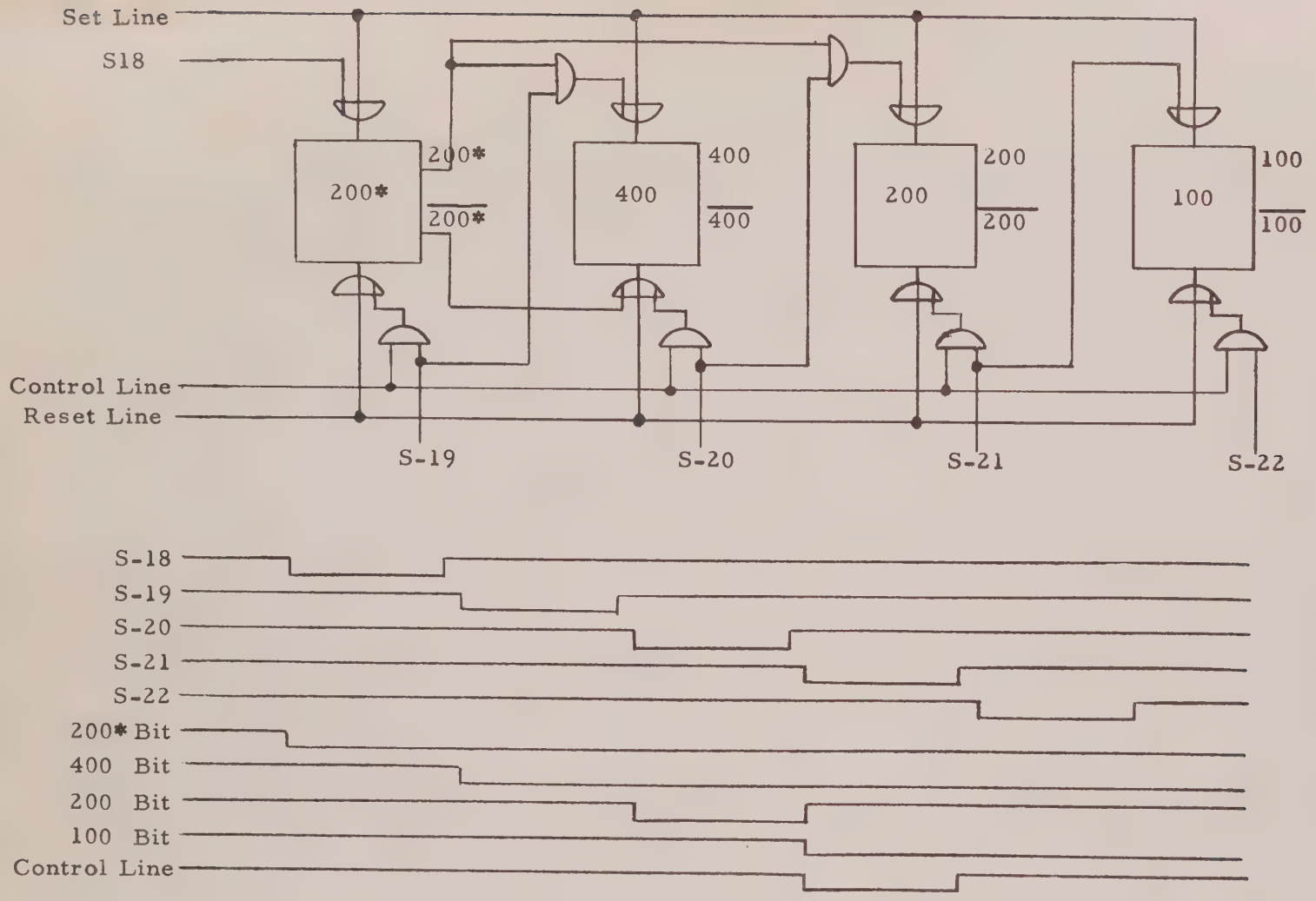


Figure 3.22. 10^2 Decade, Logic and Waveforms (Total Count = Decimal 7)

Table 3.7. Binary to Decimal Gating Logic for Unguarded Register (Any Decade)

Decimal Number (Digit)	BCD Logic
0	$\overline{2}$* $\overline{1}$
1	$\overline{2}$* 1
2	2* $\overline{4}$ $\overline{2}$ $\overline{1}$
3	2* $\overline{4}$ $\overline{2}$ 1
4	$\overline{4}$ 2 $\overline{1}$
5	$\overline{4}$ 2 1
6	4 $\overline{2}$ $\overline{1}$
7	4 $\overline{2}$ 1
8	4 2 $\overline{1}$
9	4 2 1

Table 3.8. Symbol and Decimal Point Logic for Unguarded Register

Symbol		Decimal Point Location		
Symbol	Logic	Range	Logic	Decimal Point
+	S $\overline{F1}$ $\overline{F2}$	A'	$\overline{R1}$ R2 F3	XX. XXX
-	$\overline{S}$ $\overline{F1}$ $\overline{F2}$	A	R1 $\overline{R2}$ R3	. XXXXX
~	$\overline{F1}$ F2	B	$\overline{R1}$ $\overline{R2}$ R3	X. XXXX
R	F1 $\overline{F2}$	C	R1 R2 $\overline{R3}$	XX. XXX
K	F1 F2	D	$\overline{R1}$ R2 $\overline{R3}$	XXX. XX
MV	$\overline{R1}$ R2 R3	E	R1 $\overline{R2}$ $\overline{R3}$	XXXX. X

level (from the sequencer hold inverter, board 12), the sequencer lock (from the sequencer lock flip-flop, board 12), and the lo or step inhibit signal (from the lo flip-flop, board 7). The hold and sequencer hold signals were discussed in paragraph 3.8.1. The hold signal resets the sequencer at the end of an encoding and also holds the sequencer at the output of the clock, by inhibiting the entry AND gates to the sequencer (see Figure 3.14). The sequencer hold level holds the sequencer in a manner similar to the hold signal but does not reset the sequencer (see Figure 3.14). The sequencer lock signal holds the meter sequence at sequencer step S-8 and is used in upranging only. The lo or step inhibit signal inhibits certain gates at the output of the sequencer, allowing the sequencer to count through the sequencer steps, but inhibiting the output gates associated with the measurement part of the sequence. The lo signal is an indication that the meter is within limits, and the measurement sequence is not to be performed (see paragraph 3.9).

3.9 SEQUENCER

The sequencer consists of a group of flip-flops, logically connected in order to produce changes of state in successive order (see Figures 3.14 and 3.15) after the hold signal is removed from the sequencer input. The output of the sequencer is routed through 36 consecutive gates to the program and control logic, hi-lo logic, and the register. During the measurement part of the sequence, the register increases its count with each sequencer step; however, any bit may be removed by a reject signal ($E_{fb} > E_x$) from the phase detecting circuitry at the time of the next sequencer step.

The sequencer is driven by the clock circuitry. The clock circuitry comprises a clock oscillator and a clock flip-flop. The clock oscillator produces an asymmetrical square wave at a frequency of approximately 4 KHz. The clock F.F. is driven by the clock oscillator and serves as a buffer. The clock signal is routed through a series of gates to the sequencer. The sequencer will not start however, until the hold level becomes false, and the sequencer may be inhibited after it starts by the sequencer hold signal.

When the hold line is false and the sequencer hold level is removed, pulses from both the set and reset sides of the clock flip-flop will drive the sequencer. The clock flip-flop drives the X and X' flip-flops, which in turn, drive the A and A_1 flip-flops. The true and false outputs of the A' flip-flop control the action of the sequencer. The A' signal is routed to the set input AND gate of the B flip-flop and the reset input AND gate of the C flip-flop. Conversely, the $\overline{A'}$ signal is routed to the reset input AND gate of the B flip-flop and the set input

Relay Location	Relay Number	DC										RATIO					AC				OHMS				
		Auto Filt.	w/o Filter				w. Filter			Pol.		w/o Filter			w. Filter			Auto. Filter				Auto. Filter			
		.1	1	10	100	1000	1	10	100	1000	+	-	1	10	100	1	10	100	1	10	100	1000	1K	10K	100K	1M	10M
	K-1	X	X	X	X	X	X	X	X	X			X	X	X	X	X	X	X	X	X	X					
	K-2		X	X			X	X					X			X							X	X	X	X	X
	K-3				X	X			X	X				X	X		X	X									
Inp. Func. and Range Sw. Board	K-4		X	X	X	X	X	X	X	X			X	X	X	X	X	X					X	X	X	X	X
(15)	K-6	X	X		X		X		X					X			X			X	X	X						
	K-7																			X	X	X						
	K-8																X	X		X	X	X						
	K-9						X	X	X	X						X	X	X		X	X	X	X	X	X	X	X	X
Inp.-& Filter Amp. & Null Detector	K-10		X				X	X	X	X						X	X	X		X	X	X	X	X	X	X	X
	K-11		X				X	X	X	X						X	X	X		X	X	X	X	X	X	X	X
(17)	K-12		X	X			X																				
	K-13		X				X	X	X	X						X	X	X		X	X	X	X	X	X	X	X
	K-14		X	X			X																				
	K-15											X															
Ref. Supply and Buffer Board (K16)	K-16										X		X	X	X	X	X	X		X	X	X	X	X	X	X	X
	K-17												X	X	X	X	X	X									
	K-18										X						X	X		X	X	X	X	X	X	X	X
Preamp. Bd. (18)	K-19	X																									
	K-20	X	X	X	X	X	X	X	X	X			X	X	X	X	X	X		X	X	X					
	K-21																		X								
	K-22																			X							
Ohms Atten. Board (18)	K-23																						X				
	K-24																								X		
	K-25																										X
	K-26																			X	X	X	X	X	X	X	X
Progr. Log. Bd. (12)	K-27	X					X	X	X	X						X	X	X		X	X	X	X	X	X	X	X
	K-28																										
	K-29																										
AC Conv. (19)	K-30																										
	K-31																										
Rear Rail	K-32																						X	X	X	X	X

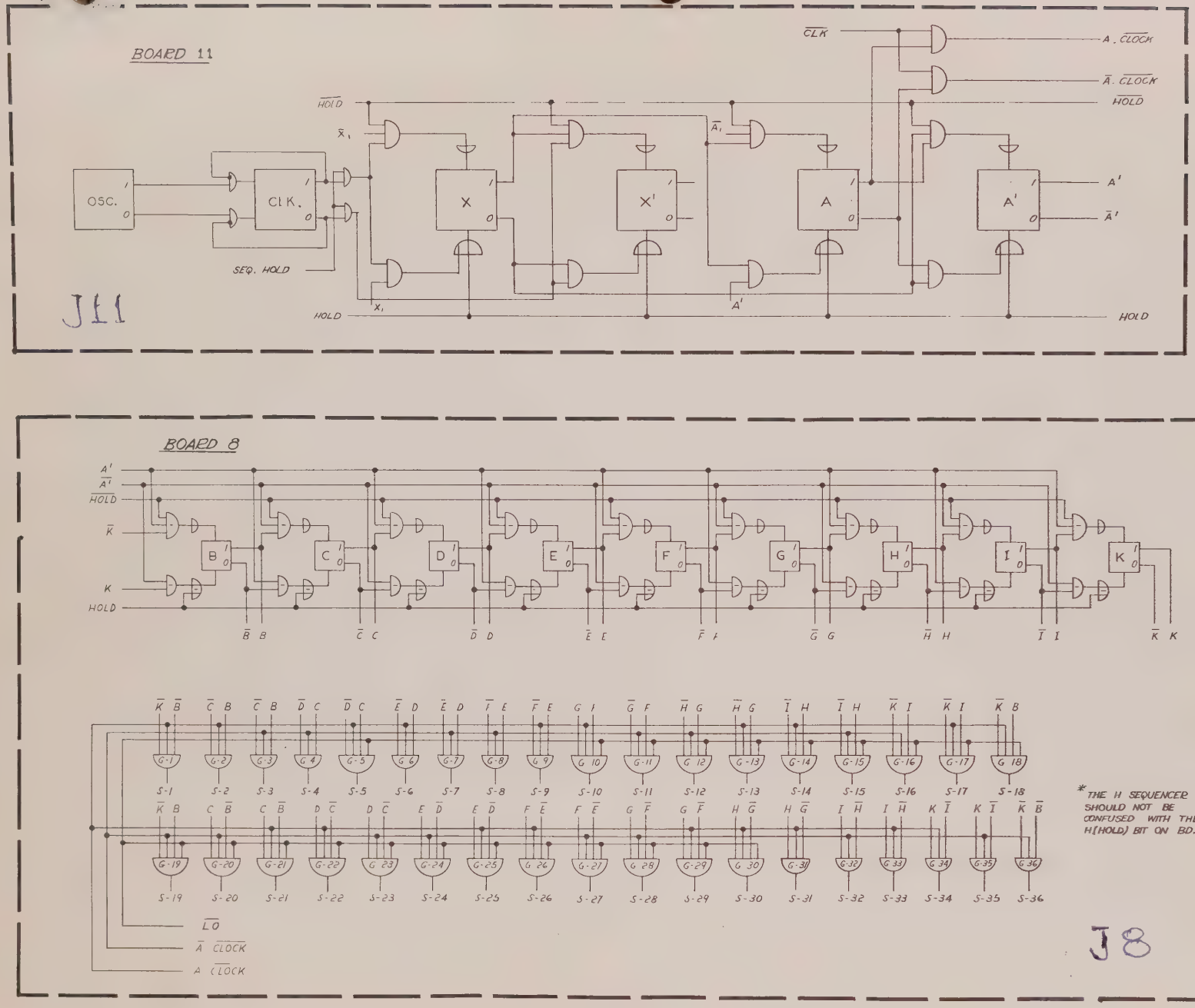


Figure 3.14. Sequencer and Sequencer Output Gates

J8 AND J11

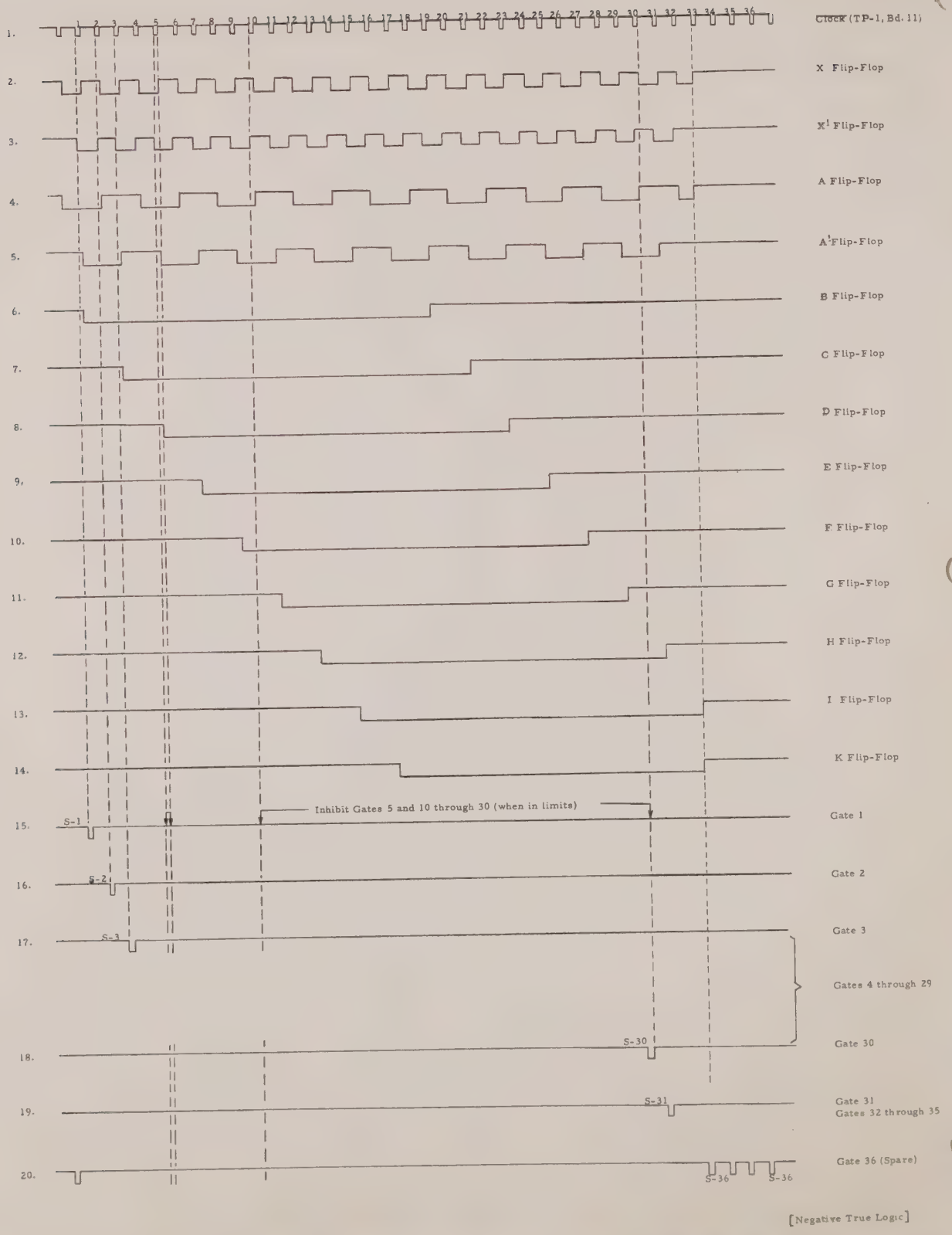


Figure 3.15. Timing Relationship of Sequencer Logic and Sequencer Output Pulses

AND gate of the B flip-flop and the set input AND gate of the C flip-flop. Thereafter, the remaining flip-flops are connected in a similar manner, with the input alternating with each successive bit. Set outputs of each flip-flop are gated with set inputs to the next successive flip-flop and reset outputs are gated with reset inputs. The configuration is such that each bit is set in succession with every alternation of the A' signal until all bits are set. Then all bits are reset in succession until step 34, at which time all remaining bits are reset simultaneously. The total number of steps is 36, however step 35 is not used. Step 36 is the reset state. The hold signal is activated at this time and the sequencer will remain in this state.

The sequencer flip-flops employ DC coupled logic. Using this type of logic, the sequencer and related circuitry are not affected by large transient signals which may occur when the meter inputs, as well as the guard, are multiplexed in a system. The outputs of the sequencer are gated at the sequencer output gates according to the gating logic in Table 3.4 (refer to Table 3.4 in conjunction with Figure 3.15). Note that each gate is satisfied only during the clock time. The time that the clock is false is allowed to prevent overlapping timing functions from satisfying more than one gate at a time.

The sequence is the series of events initiated by the 36 gated sequencer step changes and the clock pulses (see Table 3.5). The sequencer output gates are labeled G-1 through G-36 and are so arranged that at each time interval during the sequence, one gate is true allowing one clock pulse to be directed to the logic circuitry of the meter. The output pulses from these gates are called S-1 through S-36 and are referred to as the sequencer pulses. The sequencer pulses occur in numerical order; however, S-5, S-6, and S-8 may each be repetitive during range and polarity changes. Each bit of information associated with a particular sequence step is selected and interrogated (compared at the null detector) during the sequencer pulse, and acted upon (accepted or rejected) at the time of the following pulse.

Of the 36 sequencer steps, S-1 through S-3 are used for the initial hi-lo limit interrogation, S-4, S-5 and S-14 are used for downranging, S-5 and S-6 for polarity, S-6 through S-8 for upranging, S-9 through S-30 for measurement, and S-31 through S-36 for transmit and recycle.

3.9.1 Hi-Lo Limit Interrogation (S-1 through S-3)

Refer to Figure 3.16. Steps S-1 through S-3 provide for the hi-lo interrogation at the comparator (for further discussion on the action of the comparator and associated circuitry, refer to paragraph 3.7).

Table 3.4. Logic Level Input Requirements for Sequencer Output Gates (Negative True Logic)

Sequencer Output Gates	Logic Level Requirements	Sequencer Output Gates	Logic Level Requirements
1	$\overline{K}\ \overline{B}\ A\ \overline{Clock}$	19	$K\ B\ \overline{A}\ \overline{Clock}$
2	$\overline{C}\ B\ A\ \overline{Clock}$	20	$C\ \overline{B}\ \overline{A}\ \overline{Clock}$
3	$\overline{C}\ B\ \overline{A}\ \overline{Clock}$	21	$C\ \overline{B}\ A\ \overline{Clock}$
4	$\overline{D}\ C\ \overline{A}\ \overline{Clock}$	22	$D\ \overline{C}\ A\ \overline{Clock}$
5	$\overline{D}\ C\ A\ \overline{Clock}$	23	$D\ \overline{C}\ \overline{A}\ \overline{Clock}$
6	$\overline{E}\ D\ A\ \overline{Clock}$	24	$E\ \overline{D}\ \overline{A}\ \overline{Clock}$
7	$\overline{E}\ D\ \overline{A}\ \overline{Clock}$	25	$E\ \overline{D}\ A\ \overline{Clock}$
8	$\overline{F}\ E\ \overline{A}\ \overline{Clock}$	26	$F\ \overline{E}\ A\ \overline{Clock}$
9	$\overline{F}\ E\ A\ \overline{Clock}$	27	$F\ \overline{E}\ \overline{A}\ \overline{Clock}$
10	$\overline{G}\ F\ A\ \overline{Clock}$	28	$G\ \overline{F}\ \overline{A}\ \overline{Clock}$
11	$\overline{G}\ F\ \overline{A}\ \overline{Clock}$	29	$G\ \overline{F}\ A\ \overline{Clock}$
12	$\overline{H}\ G\ \overline{A}\ \overline{Clock}$	30	$H\ \overline{G}\ A\ \overline{Clock}$
13	$\overline{H}\ G\ A\ \overline{Clock}$	31	$H\ \overline{G}\ \overline{A}\ \overline{Clock}$
14	$\overline{I}\ H\ A\ \overline{Clock}$	32	$I\ \overline{H}\ \overline{A}\ \overline{Clock}$
15	$\overline{I}\ H\ \overline{A}\ \overline{Clock}$	33	$\overline{I}\ \overline{H}\ A\ \overline{Clock}$
16	$\overline{K}\ I\ \overline{A}\ \overline{Clock}$	34	$K\ \overline{I}\ A\ \overline{Clock}$
17	$\overline{K}\ I\ A\ \overline{Clock}$	35	$K\ \overline{I}\ \overline{A}\ \overline{Clock}$
18	$K\ B\ A\ \overline{Clock}$	36	$\overline{K}\ \overline{B}\ A\ \overline{Clock}$

Table 3.5. Sequence of Events

Prior to Sequence: Insert program and generate start command

S-1. Insert hi limit and reset lo limit
S-2. Reset hi limit F. F. by control line (conditional)
Set lo limit F. F. if hi is rejected
S-3. Reset hi limit F. F. if previously accepted
Reset lo limit F. F. if E_x is low (conditional)
S-4. Set 10000 (not if in manual range) (not if in limits)
* S-5. Set 00000 (not if in limits)
Set range counter to B range (DC) or A range (AC, ratio, or ohms) (conditional)
* S-6. Change polarity by control line (conditional)
Set 99999 (not if in manual range) (not if in limits)
Set up-range F. F. with trailing edge
S-7. Up range decision by control line (conditional)
* S-8. Range change complete
Reset up-range F. F. and release sequencer hold
S-9. Reset register, set 20000*
S-10. Decide 20000*, set 20000'
S-11. Decide 20000', set 20000"
S-12. Decide 20000", set 20000'"
S-13. Decide 20000'", set 10000
S-14. Decide 10000, set 200*
Downrange to A' range and reset to S-36 (conditional) (with preamplifier)
Downrange to A range (conditional) (without preamplifier)
S-15. Decide 2000*, set 4000
S-16. Decide 4000, set 2000
S-17. Decide 2000, set 1000
S-18. Decide 1000, set 200*
S-19. Decide 200*, set 400
S-20. Decide 400, set 200
S-21. Decide 200, set 100
S-22. Decide 100, set 20*
S-23. Decide 20*, set 40
S-24. Decide 40, set 20
S-25. Decide 20, set 10
S-26. Decide 10, set 2*
S-27. Decide 2*, set 4
S-28. Decide 4, set 2
S-29. Decide 2, set 1
S-30. Decide 1
S-31. Reset unguarded register
S-32. Transmit measurement to unguarded section
S-33. Generate print command
S-34. Set program flip-flop and H (hold) F. F.
S-35 Spare sequencer steps
S-36 Reset state

(* Repeatable steps)

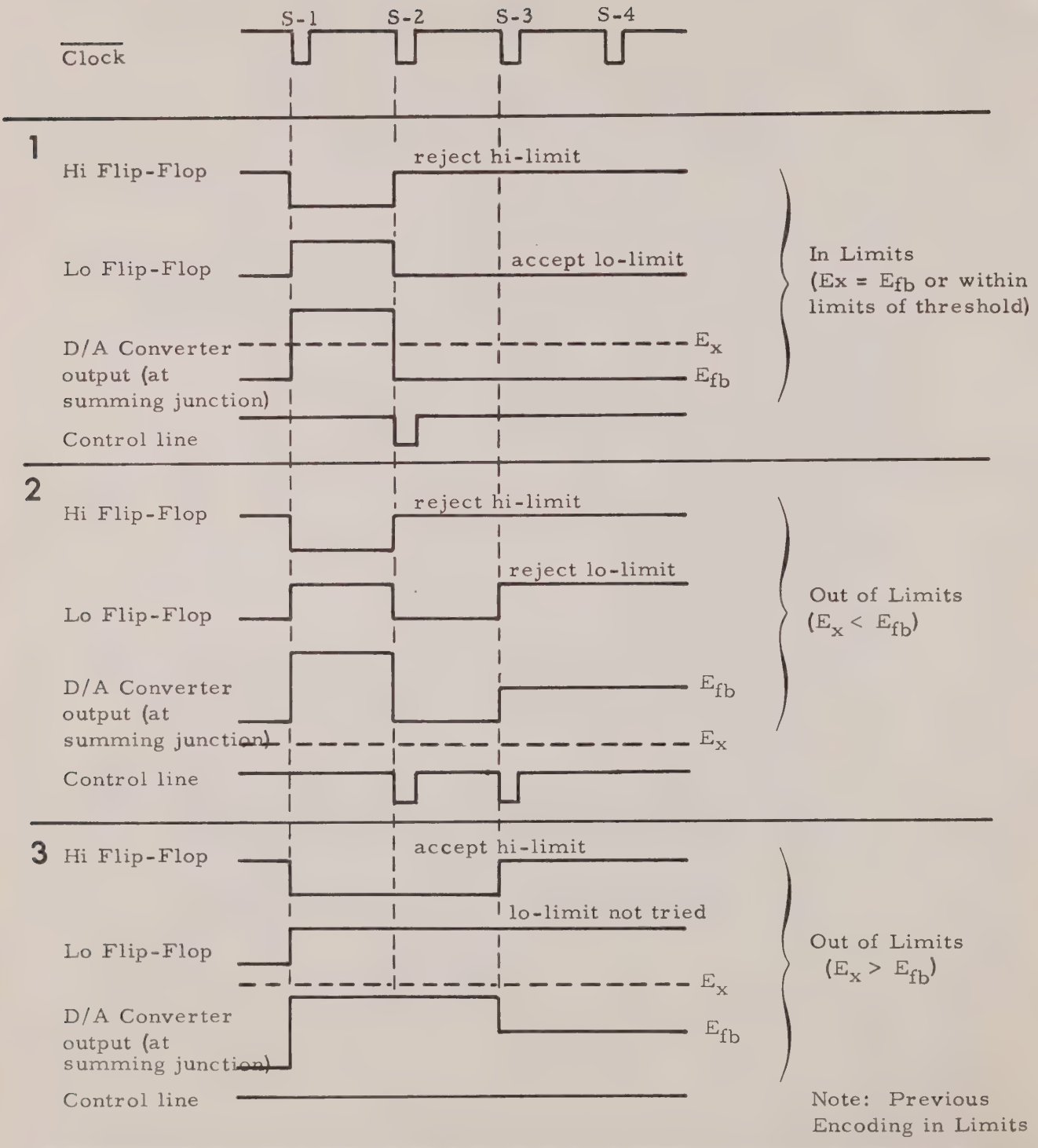


Figure 3.16. Timing Relationship of Initial Hi-Lo Limit Interrogation (S-1 through S-3)

[Negative True Logic]

This hi-lo interrogation determines whether or not the signal to be measured is identical to that from the previous encoding within one digit from that measurement. If the unknown voltage is found to be within limits (less than 1 digit change) during the initial hi-lo interrogation, the sequence is inhibited from S-4 through S-30. S-5 and S-10 through S-30 are inhibited at the sequencer output gates and S-4 and S-6 through S-9 are inhibited at gates located on the associated logic circuitry.

The first pulse (S-1) from the sequencer output gate G-1 is directed to the set side of the hi flip-flop and the reset side of the lo flip-flop. In positive polarity, the hi and S signals are routed through a positive AND gate and a positive OR gate to the NPN threshold inverter (see Figure 3.17). The output of the NPN threshold inverter is routed through the D/A converter to the comparator circuitry where it appears as a change of -2.0 mv. This voltage adds to the output of the D/A converter and is equivalent to increasing the feedback voltage by one digit.

NOTE

The polarities of E_x and E_{fb} are always opposite at the comparison circuitry. Hence, in positive polarity, E_x is positive and E_{fb} is negative, and vice-versa for negative polarity. The comparison voltages are shown in absolute (positive) voltage units in the illustrations in this manual.

In negative polarity, the S and hi signals are routed through a negative AND gate and a negative OR gate to the PNP threshold inverter. The output of the PNP threshold inverter is equivalent to increasing the feedback voltage by one digit at the comparison circuitry. If the signal to the meter has not changed by more than one digit since the last measurement cycle, as shown in example 1, Figure 3.16, the D/A converter output plus the threshold voltage will be more than E_x. If this condition exists, as it will when the same signal source is applied to the input of the meter throughout a series of measurement cycles, the reference voltage (E_{fb}) will be more than E_x. A difference signal will be generated at the output of the comparator as either an enable Z1 or enable Z2 level, depending on polarity. This difference will be gated with either the S or $\overline{S}$ bit and a control line

signal ($E_{fb} > E_x$) will be generated at S-2. The S-2 pulse then resets the hi bit and sets the lo bit. This condition creates a difference in E_{fb} opposite to that in S-1 and E_{fb} becomes less than E_x. At S-3, the comparison condition is accepted (no $E_{fb} > E_x$ pulse is generated on the control line) and the hi and lo flip-flops remain in the states set in S-2. The reset output of the lo flip-flop is used as a step-inhibit level and inhibits the measurement part of the sequence, S-4 through S-30.

If the signal input to the meter has become less than the voltage from the previous measurement by 1 digit or more (absolute value) as shown in example 2, Figure 3.16, E_{fb} will be more than E_x, the control line will generate an $E_{fb} > E_x$ signal, and the second sequencer pulse S-2 will reset the hi flip-flop and set the lo flip-flop. The feedback voltage at S-2 will continue to be rejected however, and at S-3, an $E_{fb} > E_x$ signal will reset the lo flip-flop and remove the step inhibit signal from the sequencer, allowing the measurement sequence to be performed.

If the signal has become more than the voltage from the previous measurement by 1 digit or more, as shown in example 3, Figure 3.16, a new set of conditions arises. E_{fb} will be less than E_x, and at S-2 an $E_{fb} > E_x$ signal will <u>not</u> be directed to the hi flip-flop. Thus, the feedback voltage will be accepted. Since this condition clearly indicates already that E_x is out-of-limits, the lo flip-flop is not tried and remains in the reset state. The $\overline{\text{lo}}$ output of the lo flip-flop remains true and the measurement sequence will then be performed.

NOTE

In the special case when the signal is in limits and the meter is set for a manual range that is too high for maximum resolution, there will be a zero in the 10^4 decade. As long as the meter remains in this manual range, the hi-lo interrogation will detect an in limits condition and the encoding will not be performed. However, if the meter is then set for autorange, an out of limit condition exists. At S-3, an AND gate is satisfied (see Figure 3.17), and the lo flip-flop is reset, allowing the sequence to be performed.

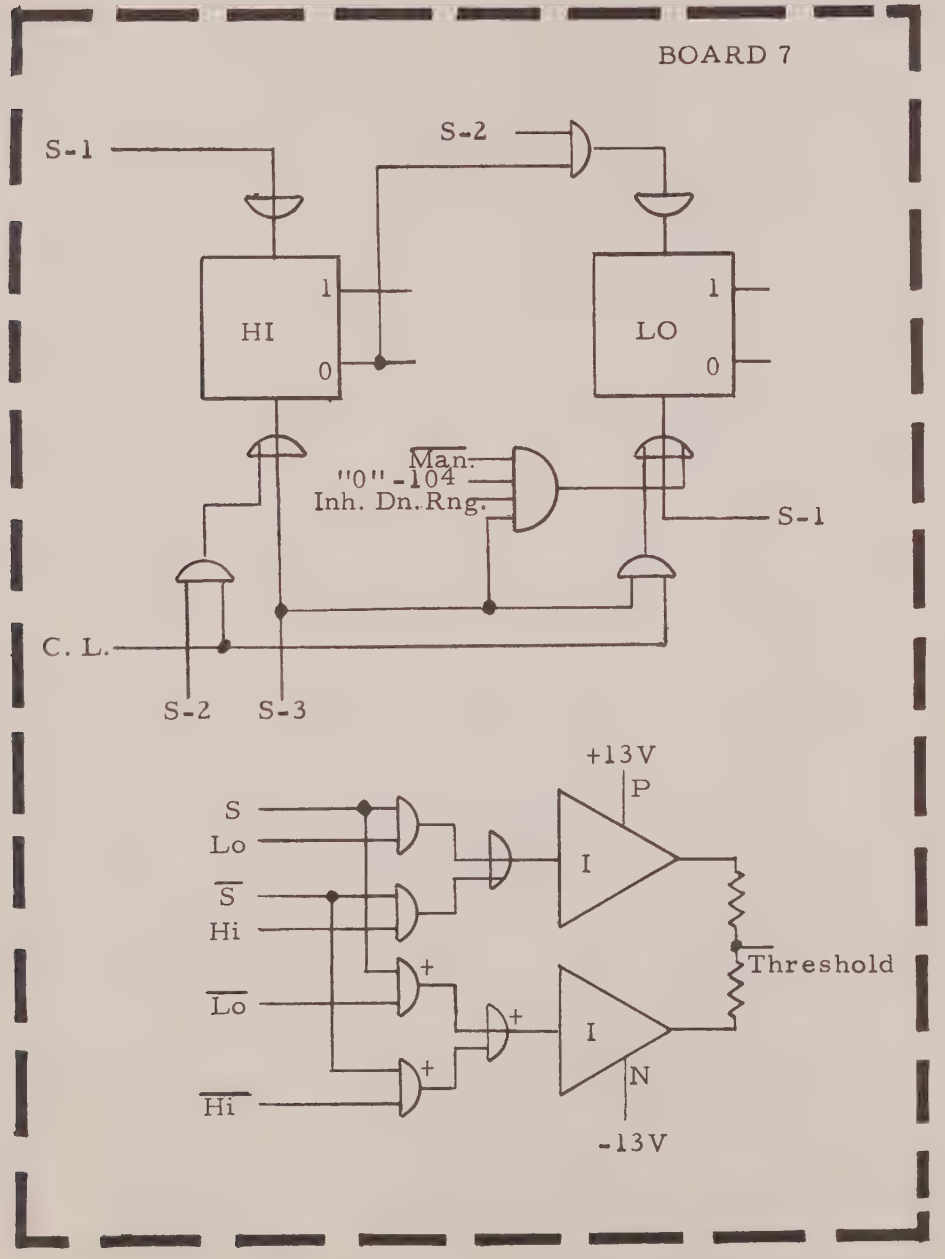


Figure 3.17. Hi-Lo and Threshold Logic

3.9.2 Downranging, Polarity Reversal, and Upranging (S-4 through S-8 and S-14)

Figure 3.18 illustrates the timing relationship of the ranging and polarity logic during sequencer steps S-4 through S-8, if downranging, polarity reversal, and upranging are all required. When any or all of these actions are not required, such as when the meter is in a manual range, etc., the sequencer is uninhibited for the corresponding step and advances immediately to the next step.

In Figure 3.18, the output of M1 is shown. When the meter is in a "filter-in" mode, mono M1 time is increased and mono M2 will also be active.

At S-4, the 10000 bit is set in the register unless one of the following conditions exists:

1. In manual range
2. In limits

At S-5, the meter downranges to B range (DC) or A range (AC, ratio or ohms) unless one of the following conditions exists:

1. In manual range
2. In limits
3. The meter is already in B range or A range, (DC, AC, ratio or ohms).
4. The meter is in A' range
5. Comparator accepts the 10000 bit

Also, at S-5, the register is reset to all 0's unless the input signal is in limits.

At S-6, the polarity of the internal reference voltage is reversed unless one of the following conditions exists:

1. In limits
2. In ratio ohms or AC
3. Comparator accepts all 0's condition

Also, at S-6, the register is set to all 9's unless one of the following conditions exists:

1. In manual range
2. In limits

At S-7, the meter decides whether to uprange or not.

At S-8, the meter upranges unless one of the following conditions exists:

1. In manual range
2. In limits
3. In highest range
4. Comparator rejects all 9's at S-7 or S-8.

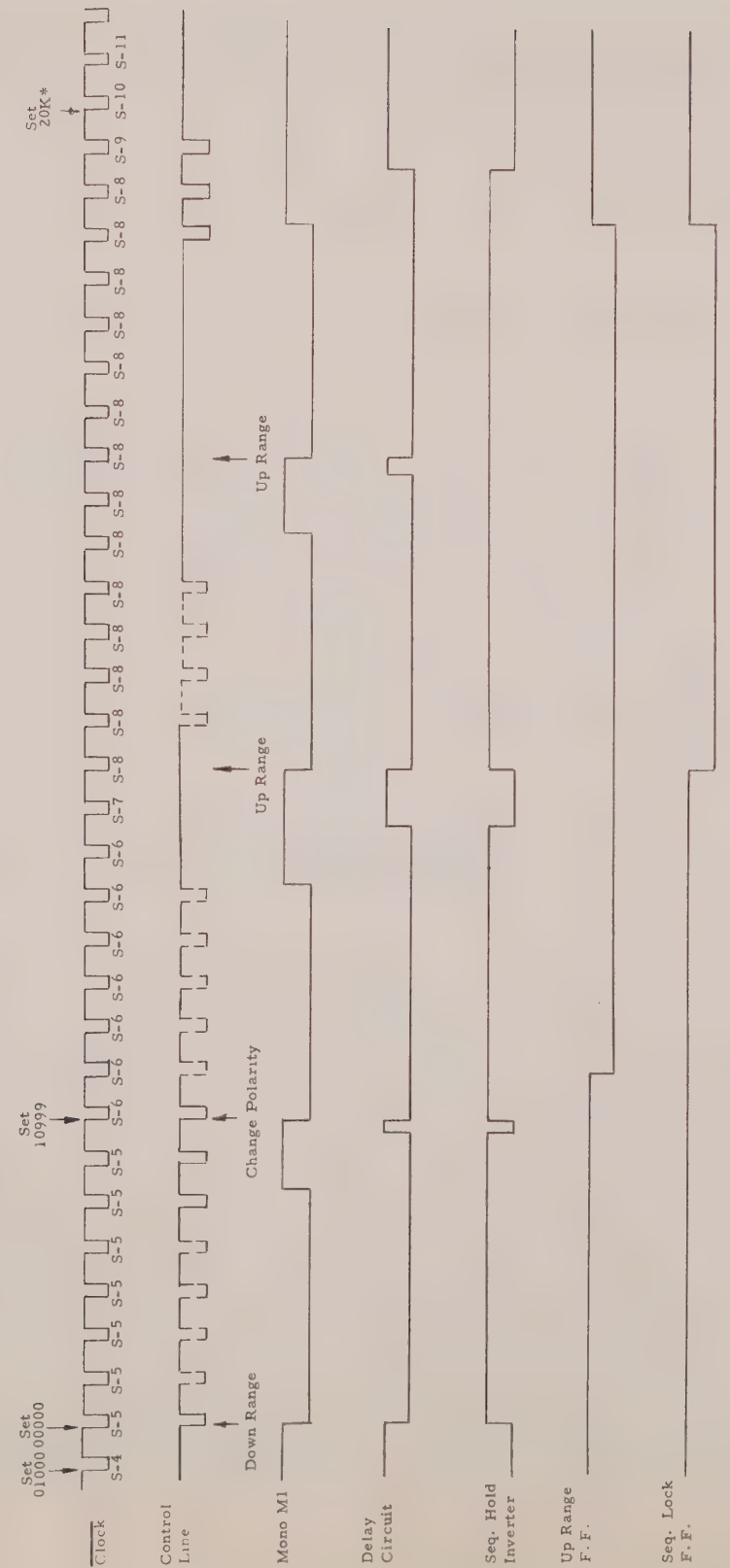

Set 01000 00000
Set 10999
Set 20K*
S-4 S-5 S-5 S-5 S-5 S-5 S-5 S-6 S-6 S-6 S-6 S-6 S-6 S-6 S-7 S-8 S-8 S-8 S-8 S-8 S-8 S-8 S-8 S-8 S-8 S-8 S-8 S-9 S-10 S-11
Clock
Control Line
Down Range
Change Polarity
Up Range
Up Range
Mono M1
Delay Circuit
Seq. Hold Inverter
Up Range F.F.
Seq. Lock F.F.

Figure 3.18. Timing Relationship of Ranging and Polarity Logic (S-4 through S-8)

At S-14, the meter will downrange to A' range (DC, with preamplifier accessory) or A range (DC without preamplifier accessory) unless one of the following conditions exists:

1. In limits
2. In manual range
3. If there is a 1 or greater integer in the 10^4 decade
4. If the meter is in AC, ohms or ratio mode

The following paragraphs describe in detail the action of the logic circuitry associated with sequencer steps S-4 through S-8 and S-14.

3.9.2.1 Downranging (S-4 and S-5)

Sequencer pulse S-4 enters the 10^4 and 10^3 decade at board 9 (see schematic at rear of test) and is gated with $\overline{lo}$ and $\overline{\text{manual range}}$ at the input of the reset emitter follower. The output of the reset emitter follower is then routed to all bits in the register (Bds. 9 and 10) and resets all bits with the exception of the 1 bit in the 10^4 decade which is set. Thus, the numerical quantity for the previous measurement is removed and the register contains 10000.

At S-5, the feedback voltage is compared to E_x at the comparison circuitry. If E_x is less than E_{fb}, a signal is generated on the control line and routed to the program logic board 12 (see schematic).

S-5 enters the program logic board and is routed to one leg of the downrange AND gate. The input requirements for this gate are S-5, $\overline{\text{manual range}}$, $E_{fb} > E_x$ on the control line, $\overline{M_2}$, and inhibit downrange. If the meter is in the lowest range for the selected mode, the inhibit downrange line will be positive; otherwise the inhibit downrange line will be negative (true). The output of the downrange AND gate is routed to M1 and also to the set lowest range line. M1 is triggered, and in turn, triggers M2 (when the meter is in the filter-in mode). The range counters are reset to B range (DC) or A range (AC, ratio or ohms). The range counters control the range relays on the input function and range switching board 16, the null detector board 17, the AC converter board 19, and the preamplifier and ohms amplifier board 18, so that the attenuators are removed and the meter in in the lowest range for direct range in DC mode, or in the AC, ratio or ohms mode.

The delay logic on the program logic board drives the sequencer hold inverter and subsequently holds the sequence until the delay signal has expired. This allows for relay closures and/or filter settling time. At the end of this time the sequencer will advance to S-6.

In the special case of measuring +DC after a measurement of negative ratio, the control line circuitry will be unable to detect a downrange requirement at sequencer step S-5, due to the reset state of the S flip-

flop remaining from the ratio measurement. If reject ($E_{fb} > E_x'$) pulses are present at S-5, they will be inhibited (see Figure 3.12). However, at the polarity reversal step S-6, when the S flip-flop reverses its state, a signal will be generated on the set lowest range line, and the meter will be in the correct range for the rest of the sequence.

3.9.2.2 Polarity (S-5 and S-6)

S-5 resets the 10000 bit and the register contains all 0's. At S-6, the feedback voltage is 0 volts, and if E_x is less than this, i.e. of opposite polarity, a signal is generated on the control line and routed to the program logic board.

S-6 enters the program logic board 12 and is routed to one leg of the polarity AND gate. The input requirements for this gate are S-6, $\overline{lo}$, $\overline{F_2}$ (DC or ratio), $\overline{up\ range}$, $\overline{M_2}$, and $E_{fb} > E_x$ on the control line. When the polarity AND gate is true, a pulse is routed to M1, firing M1, and also firing M2 in succession when applicable (filter-in modes). The combination of M1, $\overline{uprange}$, S-6 and either Z1 or Z2 and $\overline{F_2}$ changes the state of the S (polarity) flip-flop. The output of the S flip-flop selects the appropriate symbol (+ or -) in the symbol readout for the DC mode. The S or $\overline{S}$ logic level is gated with the mode logic level on the range and function logic board, and the gated signal thus produced is applied through relay drivers to appropriate relays in the reference supply. In the positive polarity, relays K16 and K18 are energized, selecting a negative reference voltage. In the negative polarity, relay K15 is energized, selecting a positive reference voltage.

When measuring negative ratio, i.e. comparing a negative signal voltage with a negative external reference, the S bit is reset at S-6, but the symbol readout and the buffer amplifier switching relays are unaffected. The output of the buffer amplifier will be positive and the comparison circuitry will operate the same as for negative DC.

The delay logic on the program logic board, M1 or M1 and M2 (filter-in mode), drives the sequencer hold inverter and subsequently holds the sequence until after the last mono pulse has expired. This allows for relay closures in the buffer amplifier and filter settling time (when applicable). At the end of the last mono time the sequencer will advance to S-7.

3.9.2.3 Upranging (S-6 through S-8)

Refer to Figure 3.19. S-6 enters the 10^4 and 10^3 decade board 9 and is routed to the set line emitter follower. At the input of the set line

emitter follower, S-6 is gated with $\overline{\text{lo}}$ and $\overline{\text{manual range}}$. The output of the set line emitter follower is routed to the register (boards 9,and 10,) and sets an all 9's condition (see Figure 3.21 and 3.22).

S-6 also enters the program logic board 12, and the trailing edge of S-6 sets the uprange flip-flop, preparing the meter for upranging (see Figure 3.12).

At S-7 the feedback voltage is compared to E_x and if E_x is greater than E_{fb} an upranging condition exists and no signal is generated on the control line. The uprange flip-flop remains in the set state. If E_x is less than E_{fb}, no upranging condition exists, and an $E_{fb} > E_x$ signal is generated on the control line and routed to the program logic board 12. The coincidence of $E_{fb} > E_x$ on the control line, $\overline{M_2}$, $\overline{M_1}$, and S-7 resets the uprange flip-flop. Also, if the range counter is already in the highest range (for the particular mode), true level is developed on the reset up-range line (see Figure 3.13) and routed to the program logic board. At coincidence with S-7, this signal will also reset the uprange flip-flop, since further upranging would be impossible.

S-8 is brought into the program logic board and routed to the input AND gate of the sequencer lock flip-flop and to the uprange AND gate. The input AND gate of the sequencer lock flip-flop requires the combination of logic levels S-8, up-range, and $\overline{\text{lo}}$ or $\overline{\text{manual range}}$ for a true output. A true output from this gate sets the sequencer lock flip-flop. The output of the sequencer lock flip-flop turns on the sequencer hold inverter holding the sequence at S-8.

The combination of $\overline{\text{delay}}$ and the output of the sequencer lock input AND gate satisfies the uprange AND gate, triggering M1. M1 and the set output of the sequencer lock flip-flop are gated at the range counter (range logic board 13) and the gated signal is routed through the uprange inverter to increase the setting of the range counters by one range (see Figure 3.13). The range counters, in turn, control the range relays on the input function and range switching board 15, the AC converter board 19 or the preamplifier and ohms amplifier board 18 and the null detector board 17, and select the attenuator corresponding to the next higher range.

At the expiration of M1, mono M2 will be triggered if the meter is in a filter-in mode. After monos M1 and M2, and the delay circuit are reset, the sequence will remain at S-8, since the sequencer lock flip-flop is set and the sequencer hold inverter is turned on. The sequencer lock flip-flop is reset only when the uprange flip-flop is reset.

The reset output of the delay circuit is routed to the uprange AND gate, and at the end of the delay time, mono M1 will be triggered and the uprange cycle repeated unless the uprange flip-flop has been reset pre-

viously by the control line or by the reset uprange line. As long as a false level is present on the control line, the unknown voltage Ex is more than Efb, and the uprange circuitry will recycle and the range attenuators will increase one range during each delay time. As long as a false level is present on the reset uprange line, the meter is not in the highest range (for the particular mode). When E_x becomes less than E_{fb} , the meter is in the proper range, and a signal on the control line is gated with $\overline{M}_2$, $\overline{M}_1$ and S-8 and resets the uprange flip-flop. Or, if the range counter reaches the highest range for the particular mode, a signal on the reset uprange line is gated with S-8 and resets the uprange flip-flop regardless of the control line decision. In either case, when the uprange flip-flop is reset, the reset output resets the sequencer lock flip-flop, thus relieving the sequencer hold and allowing the sequencer to continue to the next sequencer step S-9.

3.9.2.4 Downrange (S-14)

In the DC mode, when the preamplifier is not installed in the meter, the instrument will downrange to A range and reset the sequencer if there is a "0" in the 10^4 decade at S-14. A "0" in the 10^4 decade is is an indication that the full five digit resolution of the instrument is not being utilized and downranging is necessary. This condition overrides any control line decision at S-14.

When the preamplifier board is removed from the instrument, a connection between pins 7 and 8 and between pins 9 and 10 are broken on board 18 (see schematic at rear of text). The disable A and enable A' lines in the instrument are then floating and any AND gate requiring either of these signals sees a true input. Any OR gate sees a false input.

Refer to Figures 3.12 and 3.13. S-14 is gated with the reset output of the downrange lock flip-flop, and the gated signal is true on the S-14 out line. An AND gate on the range and function logic board 13 is satisfied by B range, R_2 , R_3 , DC, $\overline{\text{manual range}}$, S-14 out, and "0"-$10^4$. The output of this AND gate triggers M1 and is also gated with M1 and disable A to reset the range counters to A range. At the expiration of M1, M2 is triggered and there is an appropriate delay. When the A range is set, the A and disable A logic levels are gated with M1 and S-14 out and set the hold flip-flop, resetting the sequencer to S-36. The S-14 signal is also used to set the down range lock flip-flop, to prevent further downranging at S-14. At the end of the delay time, the hold flip-flop is reset and the sequencer immediately starts S-1 and continues through the sequence. Since the meter is presuma- in the correct range at this time, S-1 through S08 have no effect.

However if the signal does change during this time, the ranging and polarity sequence will be performed again, as described in the previous paragraphs.

When the preamplifier board is installed in the instrument, the disable A line is positive (false) and the enable A' line is negative (true). S-14 is gated with the reset output of the downrange lock flip-flop, and the gated signal is true on the S-14 out line. An AND gate on the range and function logic board 13 is satisfied by enable A', R_2 , R_3 , DC, manual range, S-14 out, and "0"-10^4 . The output of this AND gate triggers M1 and is also gated with M1 and enable A' to reset the range counters to A' range. At the expiration of M1, M2 is triggered and there is an appropriate delay. When the A' range is set, the A', M1 and S-14 out logic levels are gated and set the hold flip-flop, resetting the sequencer to S-36. The S-14 signal is also used to set the downrange lock flip-flop, to prevent further downranging at S-14. At the end of the delay time, the hold flip-flop is reset and the sequencer immediately starts S-1 and continues through the sequence. At the upranging sequencer step S-8, the feedback voltage is interrogated, and the meter will uprange to A range, if required.

3.9.3 Measurement (S-9 through S-30)

The timing relationship of the measurement sequence for the first two decades is illustrated in Figure 3.20; the following decades would appear in a similar manner. The first or 10^4 decade of the register is arranged according to a 2*2'2"2"' 1 code; all other decades are in a 2*421 code (see paragraph 3.10 for a description of the register). When a bit in the register is selected, a corresponding increase in voltage at the output of the D/A converter is felt at the comparison circuitry. As each bit is inserted into the register, the feedback voltage at the comparison circuitry is also increased, until the feedback voltage is greater than E_x . At that time, a reject or E_{fb} E_x pulse is routed by control line back to the register, removing the previous bit. Refer to paragraph 3.7 for a description of the comparator and null detector circuitry.

In Figure 3.20 an example signal voltage E_x of +3.7000V is to be measured. Sequencer pulse S-9 is gated with lo on the 10^4 and 10^3 decade board and a reset pulse is generated (see Figure 3.19). The reset pulse is routed to the reset inputs of all bits in the guarded register except for the 2* bit in the 10^4 decade. S-9 and lo are gated at the set input of the 20K* bit (see Figure 3.21). Thus, the 20K* bit is set and all other bits are reset. At S-10, the comparator circuitry accepts the 20K* bit, since the resulting analog voltage at the E_{fb} side of the comparator (2 volts) is less than 3 volts (the most significant digit of E_x).

Sequencer pulse S-10 sets the 2' bit in the 10^4 decade of the register. At S-11, the comparator circuitry rejects the feedback voltage E_{fb} (which is now 4 volts), and an E_{fb} E_x signal is routed by control line

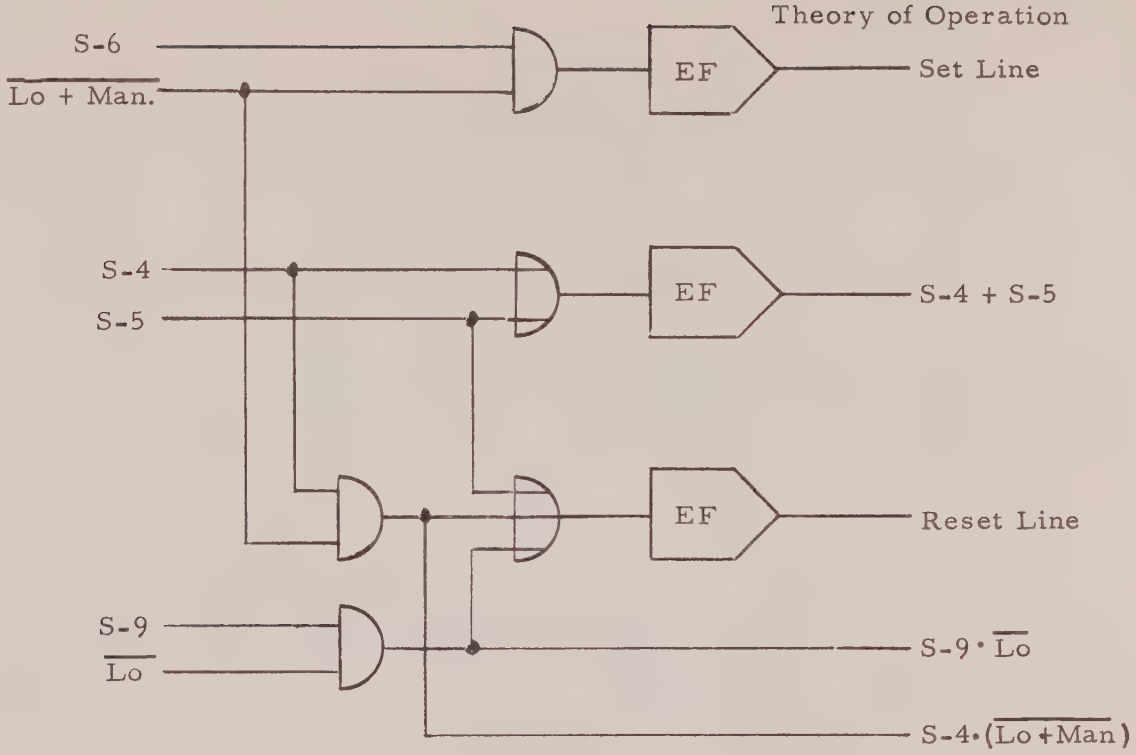


Figure 3.19. Set Line and Reset Line

to the register, removing the 2' bit and reducing E_{fb} back to 2 volts. Since a 2 bit was rejected, the following two bits (2'' and 2''') are not tried and the feedback voltage E_{fb} remains at 2 volts. Sequencer pulses S-11 and S-12 are inhibited at the input of the register.

S-13 sets the 1 bit in the 10^4 decade. At S-15, the comparator circuitry accepts E_{fb} (3 volts) which is less than E_x (3.7000 volts) and in addition, the 2* bit in the 10^3 decade is set.

NOTE

Since there is not a zero in the 10 decade for the example signal voltage used, the meter continues on to S-15. However, if there was a 0 in the 10^4 decade at this time, the range counter would be set to the A' range and the sequencer would be set to S-1 (with preamplifier accessory) or the range counter would be set to the A range (without preamplifier accessory). See paragraph 3.9.2.4.

Also at S-15, the 4 bit in the 10^3 decade is set, increasing E_{fb} to 3.6000 volts. This feedback voltage is accepted at S-16 and the 2 bit is set. At S-17, the comparator circuitry rejects E_{fb} (3.8 volts) which is more than E_x (3.7000 volts). The 2 bit is removed (reset)

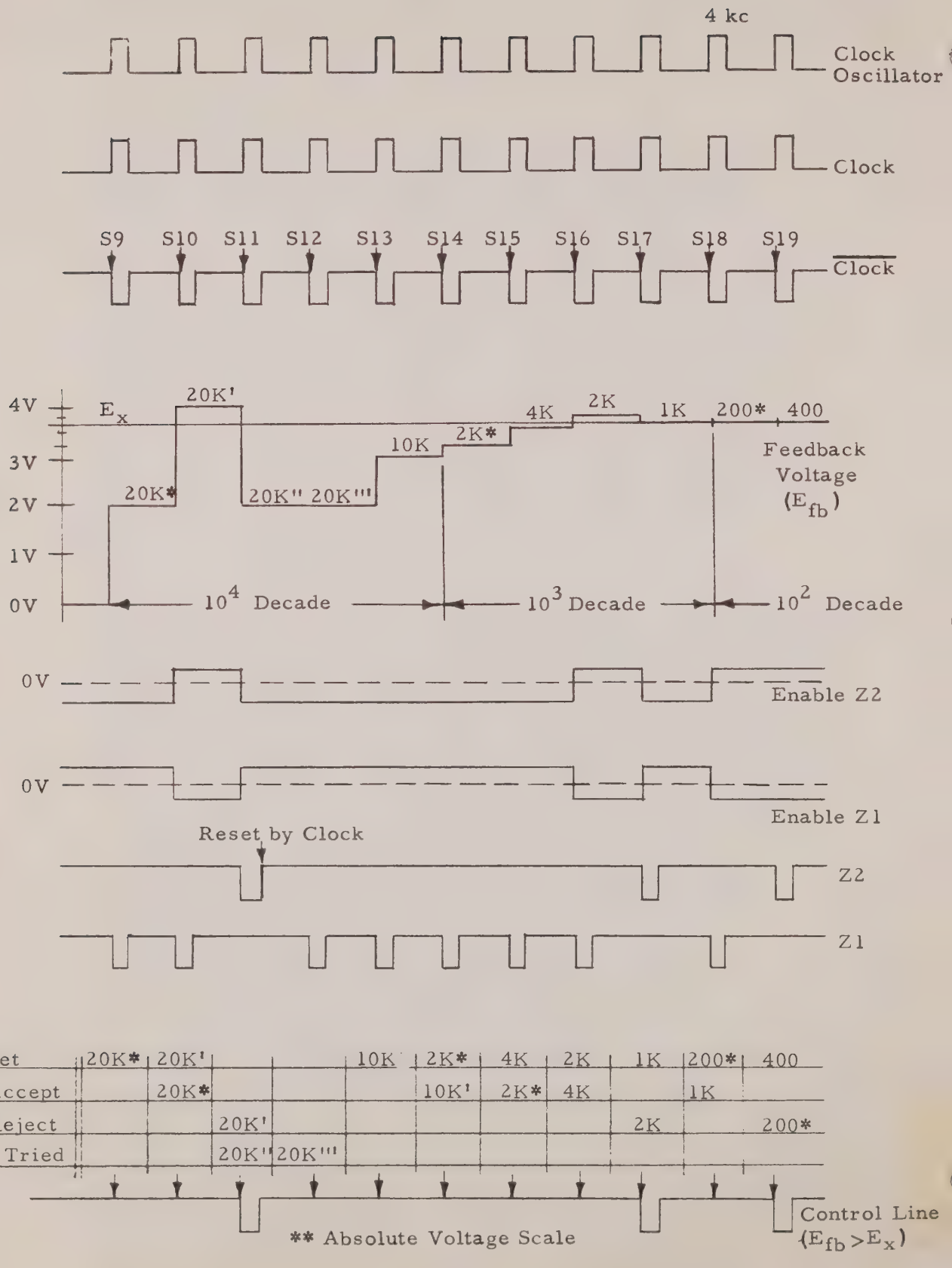


Figure 3.20. Timing Relationship of Clock Circuits and Measurement Sequence (E_X = +3.7000V)

and the 1 bit is set. At S-18, the 1 bit is accepted since $E_{fb} = E_x$. All following bits will be tried (set) and rejected (reset) since the remaining digits of E_x are equal to 0.

3.9.4 Reset Unguarded Register, Transmit to Unguarded Section, and Print (S-31 through S-33)

S-31 is directed across the guard and resets the unguarded register. S-32 is routed to the program logic board 12 and is then directed through an emitter follower and a driver (see Figure 3.12). The output of the driver is used as a transmit signal, and is applied to the guard. The measurement magnitude and program information is then transferred simultaneously across the guard. S-32 also resets the manual range flip-flop and the downrange lock F.F. The trailing edge of S-33 is routed across the guard as a print command. The print command sets the print flip-flop on the outside power supply and control logic board 1. The set output of the print flip-flop is routed through an emitter follower, to the rear panel connectors J102 and J103. This signal can then be used to command an external printer or similar recording device.

3.9.4.1 Guard Crossing

The guarded to unguarded section guard crossing circuitry (board 6 to board 5) contains 5 program lines (3 range and 2 mode), 20 measurement magnitude lines (in binary code), one polarity line, a reset line, a transmit line, and a print line. The program, measurement magnitude, and polarity lines require a negative enable. The reset, transmit, and print signals are in the form of positive going edges. In contrast to the unguarded to guarded section guard crossing (see paragraph 3.4.2.3), only the set or true lines are used. The information contained on the program, measurement magnitude and polarity lines are all transferred simultaneously across the guard when the transmit line becomes true at S-32. The reset and print lines are separately connected and these logic levels cross individually at S-31 and the end of S-33, respectively. The coils in the unguarded section are connected in reverse to those in the guarded section, so that the program and measurement logic is inverted from positive to negative pulses in crossing the guard. This inversion makes the logic compatible with the NPN type transistors used in the unguarded program logic circuits and unguarded register.

3.9.4.2 Transmit Program Information

The program logic circuitry is discussed in paragraph 3.8.2. The set outputs of the program flip-flops are connected to the guard gating circuitry at board 5 and enable their respective gates. At S-32, the transmit line becomes positive and the gates are triggered, inducing

negative pulses in the guard transformer coils. The range information determines the decimal point placement. The mode information (F1 and F2), in conjunction with the polarity bit (S) determines the symbol indication (+, -, ~ , K, or R). The millivolt lamp is lighted when the meter is in the DC mode and A' range (see Table 3.8).

3.9.4.3 Transmit Measurement Information

The guarded register is discussed in paragraph 3.10. As described in paragraph 3.10, the first or 10^4 decade uses a special code and all other decades use the standard 2*421 code. The set outputs of the 10^4 decade are routed to decoding gates on the same board. The decoding gates convert the special code to the 2*421 code. The outputs of these gates, along with the set outputs from the 10^3 through 10^0 decades of the register, are routed to the guard gating at board 6. When the transmit line becomes true at S-32, the measurement magnitude is transmitted across the guard to the unguarded register.

3.9.5 End of Sequence (S-34 through S-36)

S-34 is routed to the program logic board and sets the program flip-flop and the hold flip-flop. The set output of the hold flip-flop resets the sequencer to S-36. S-35 is a spare sequencer steps, not used in this instrument. S-36 is the reset state of the sequencer, and the output of gate G36 is not used in the meter logic. Since the hold bit is set at S-34, the sequencer is prevented from continuing through another sequence. S-36 pulses will then be generated with each clock pulse until the start of the next sequence. If S-34 is bypassed and the hold bit is not set, as in the case when the meter enters the A' range at S-14 and immediately resets the sequencer to S-36, the following pulse from the clock sets the A bit and the sequence of the meter proceeds to S-1.

3.10 GUARDED REGISTER

The guarded register is made up of five decade stages, 10^4 through 10^0 . The first, or 10^4 decade comprises five flip-flops corresponding to the binary digits 2*2'2''2''' and 1. The remaining decades have four flip-flops each and are arranged according to a 2*421 code. The numerical value of each selected bit is effectively added in each decade, and the sums of all decades are added according to the factor each represents to make up the total decimal number (see Table 3.6). The powers of ten representing the decades designate the placement of individual digits starting with the "ten thousands" digit and ending with the "units" digit. The maximum decimal count for each decade is 9, i.e.

when all flip-flops are set.

The decimal count contained in the register is controlled by the sequencer and control line (described below). The register performs two functions: it controls the analog voltage output of the D/A converter, and at the end of an encoding, stores the measurement magnitude in binary code. At sequencer step S-32 this measurement magnitude is transferred across the guard and similarly stored in the unguarded register. The unguarded register then routes this information to the Nixie drivers and to the remote connectors on the rear panel.

The 10^4 and 10^3 decades of the guarded register are illustrated in Figure 3.21. The 10^2 decade and waveforms are illustrated in Figure 3.22.

The inputs to the set and reset sides of each register bit are DC coupled OR gates. On the set side of each bit, one input to the OR gate is the set line (which is used to set the upranging point in the register at sequencer step S-6). The other input is the sequencer pulse line corresponding to that bit. On the reset side, one input to the OR gate is the reset line. The reset line is used at sequencer steps S-4, S-5, and S-9 to completely or partially reset the register (depending on program and logical decisions). The other input is taken from an AND gate, which is satisfied by the control line ($E_{fb} > E_x$) and the sequencer pulse corresponding to the next successive bit. When a bit is rejected by the comparator circuitry, it is removed, or reset, by the next sequencer pulse.

Redundant bits in each decade are logically connected to prevent ambiguous codes from resulting after repeat comparisons at the chopper. If the first 2 bit in the 10^4 decade is tried, and then rejected, no other 2 bits in that decade will be selected. Or, if the 2* bit in the 10^3 decade is tried and rejected, the 2 bit will not be tried. For example, suppose that the input signal E_x is 1.9999 volts. Sequencer pulse S-9 will select (set) the first 2 bit in the 10^4 decade. At S-10, this bit will be rejected (reset) and no other 2 bit will be tried. If the bits were all tried however, and the signal input voltage changed to more than 2 volts at S-10 (or at one of the two following sequencer pulses), a 2 will have been rejected once and another two will be selected. Thus, an ambiguous code would result which the decimal decoder gates in the unguarded section could not recognize.

Paragraph 3.9.3 describes the method of selecting and rejecting bits in the register when an example input voltage of 3.7000 volts is applied to the meter.

To illustrate the timing relationship of the individual bits as related to the sequencer pulses, an example count of 7 is entered into the 10^2 decade in Figure 3.22. This decimal value would correspond to the "hundreds" digit of the input signal. As shown in the figure, the 2*, 4 and 1 bits are accepted, while the 2 bit is rejected. The summation of individual bits equals the decimal 7 (the actual conversion to an analog voltage is made at the D/A converter). Note that the 2 bit is rejected at the same time the 1 bit is selected.

3.11 UNGUARDED REGISTER

The unguarded register is made up of five decade stages for the measurement magnitude and six program flip-flops (bits) for the program information. The five decade stages store the measurement magnitude in 2*421 code and are similar to the 10^3 through 10^0 decades of of the guarded register, except that all logic in the unguarded register is positive true. The 10^4 decade and program bits are contained on the 10^4 decade and Nixie driver board 2, the 10^3 and 10^2 decades are on board 3, and the 10^1 and 10^0 decades are on board 4 (see appropriate schematics). Note that decade boards 3 and 4 are identical.

When the program and magnitude information is transmitted across the guard it is routed directly to the unguarded register and the appropriate bits are set. The unguarded register remains in this state until S-31 of the next encoding, so that the information is stored and can be obtained from the rear panel connectors J-101, J-102, and J-103 during this time. The outputs of the register are also routed through decoders to Nixie driver transistors.

Refer to Table 3.7 for gating logic. Each measurement decade of the unguarded register is connected so as to avoid ambiguous codes. The clamping diodes are connected from the set output of the 2* bit to the set outputs of the 4 and 2 bits. When the 2* bit is false, the negative output clamps the outputs of the 4 and 2 bits so that the 4 and 2 bits are effectively false also. Only when the 2* bit is true may the 4 or 2 bits be set.

Refer to Table 3.8. Program bits are gated according to the program logic codes and control the symbol readout and the neon lamp decimal points. For example, the + symbol is displayed in the readout when S bit is true (positive polarity), and the F1 and F2 logic levels are false (DC mode). The B range decimal is lighted when R3 is true and R2 and R1 are false.

Table 3.6. Binary to Decimal Conversion Chart for the Guarded Register

Decimal	Register Bit			
	2*	4	2	1
0	0	0	0	0
1	0	0	0	X
2	X	0	0	0
3	X	0	0	X
4	X	0	X	0
5	X	0	X	X
6	X	X	0	0
7	X	X	0	X
8	X	X	X	0
9	X	X	X	X

10^4 Decade

Decimal	Register Bit				
	2*	2'	2''	2'''	1
0	0	0	0	0	0
1	0	0	0	0	X
2	X	0	0	0	0
3	X	0	0	0	X
4	X	X	0	0	0
5	X	X	0	0	X
6	X	X	X	0	0
7	X	X	X	0	X
8	X	X	X	X	0
9	X	X	X	X	X

X = Set or True State 0 = Reset or False State

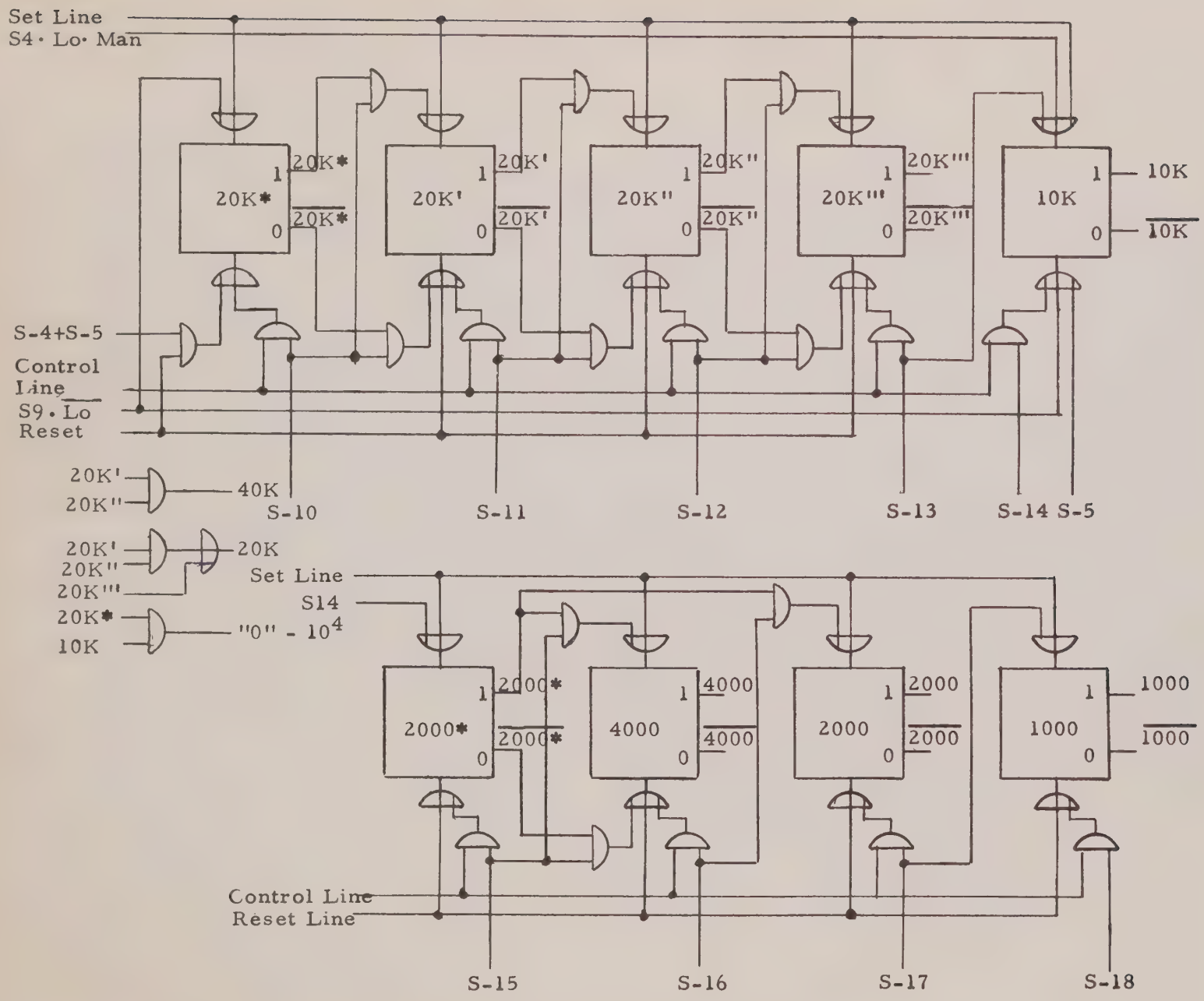


Figure 3.21. 10^4 and 10^3 Decades in Guard

3.12 NIXIE DRIVERS AND READOUT

The outputs of the five magnitude decade stages and program bits are routed to the rear panel connector J-101 (BCD outputs) and also through decoding gates to Nixie driver transistors where the 2*421 binary codes are converted to 10-line decimal codes and the program codes are converted to individual program outputs. The outputs of the magnitude decade stages are also routed through decoding gates (2*421 to 8421) to correspondingly labeled board terminals; however, the 8421 outputs are not normally wired to the rear panel connector unless the meter is specifically ordered that way or the meter is modified in the field.

The Nixie driver outputs are routed both to the Nixie tubes on the front panel and to the rear panel connectors J-101 and J-102 for 10-line decimal and individual program outputs. One magnitude decade and the Nixie driver configuration is illustrated in Figure 3.22. The numbers in the Nixie drivers correspond to the numbered cathodes of the Nixie tube. For an example, the decimal number 3 is entered into the decade. All true outputs of the register are circled in the illustration. The entry AND gate to the number 3 Nixie driver is satisfied and a ground level is routed to the number 3 cathode of the Nixie tube, lighting that number. The symbo l and decimal point drivers (not shown) operate in a similar manner as the magnitude drivers.

3.13 POWER SUPPLIES - GUARDED AND UNGUARDED SECTIONS

The power supply for the unguarded section is located on the outside power supply and control logic board 1. Three bridge rectifiers supply -15V, +15V, and +230V. The -15V and +15V supplies are regulated and supply the potentials for the transistor logic in the unguarded section. The +230 volt supply is unregulated and supplies the voltage to light the Nixie tubes. A +70 volt potential is obtained from the +230V supply through a voltage divider, and is used as a bias voltage in the unguarded section.

The power supply for the guarded section is contained on the power supply board 7 and the capacitor bracket (located at the inside rear of the instrument). Three regulated bridge rectifiers supply +13V, -45V and +45V. In addition, -13V is obtained from the -45 volt supply through a zener regulated voltage divider. The -13V, and -45V supplies are zener regulated. The +13V and +45V supplies are regulated by the -13V and -45V supplies, respectively. The +13V, -13V and -45V supplies provide the voltages for the guarded transistor logic. The +45V supply is used as bias potentials.

SECTION IV

CALIBRATION

4.1 CHECKOUT PROCEDURE

This checkout procedure verifies that the instrument is in good operating condition. If the instrument does not respond properly, refer to the calibration procedure, paragraphs 4.2, 4.3, and 4.4. To make the tests, a DC voltage source variable from 0 to 1000 volts; a precision 10V DC reference voltage source; an AC voltage source variable from 0 to 750V RMS, and a precision potential divider (Dekavider or equivalent) are required. The output of the potential divider and DC source combination must be adjustable in steps of 1 microvolt. Refer to Figures 4.1 through 4.4 for test setups.

a. Set the instrument front panel switches as follows:

POWER	ON (Allow fifteen minutes warmup)
ENCODE	CONT
MODE	DC
RANGE	AUTO
FILTER	OUT

b. Connect the signal inputs to the meter for DC measurements as illustrated in Figure 4.1.

c. Adjust the DC voltage standard for an output between .1 and 1 volt, 1 and 10 volts, 10 and 100 volts, and then between 100 and 1000 volts. If the preamplifier is installed in the meter, adjust the DC voltage standard for an output of between 0 and .1V. The meter will range automatically to the correct range and read the correct voltages and polarity.

d. Adjust the DC voltage standard for an output of close to 10 volts and note the value and polarity of the reading. Then reverse the polarity of the input signal. The meter will give the same value of reading ±1 digit with opposite polarity indication.

e. Set the RANGE switch successively to the .1V (with preamplifier accessory), 1V, 10V, 100V, and 1 KV positions. In each case, apply a voltage to the meter within the range selected. Check that the voltage, range and polarity indications are correct within the specified tolerances (paragraph 1.7).

f. Set the RANGE switch to the 10V position and apply a voltage slightly higher than 10 volts to the meter. The meter will read 9.9999.

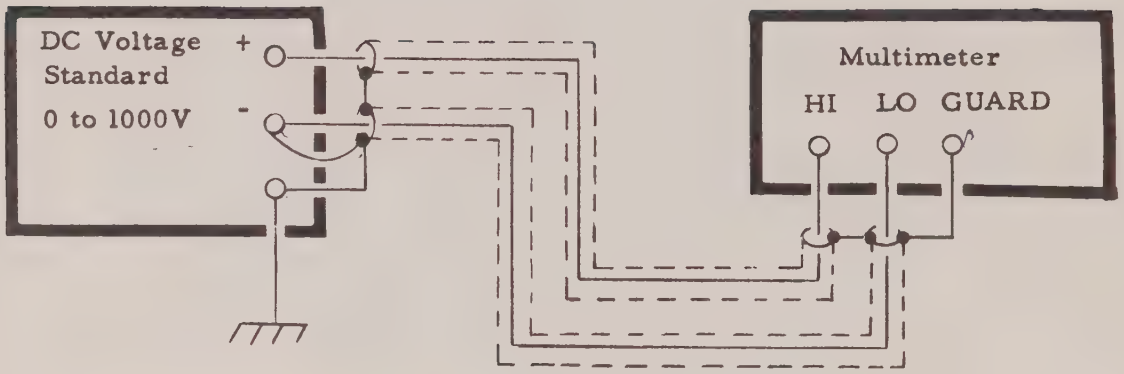


Figure 4.1. Precision DC source Input Connections for Checking DC Volts Measurements

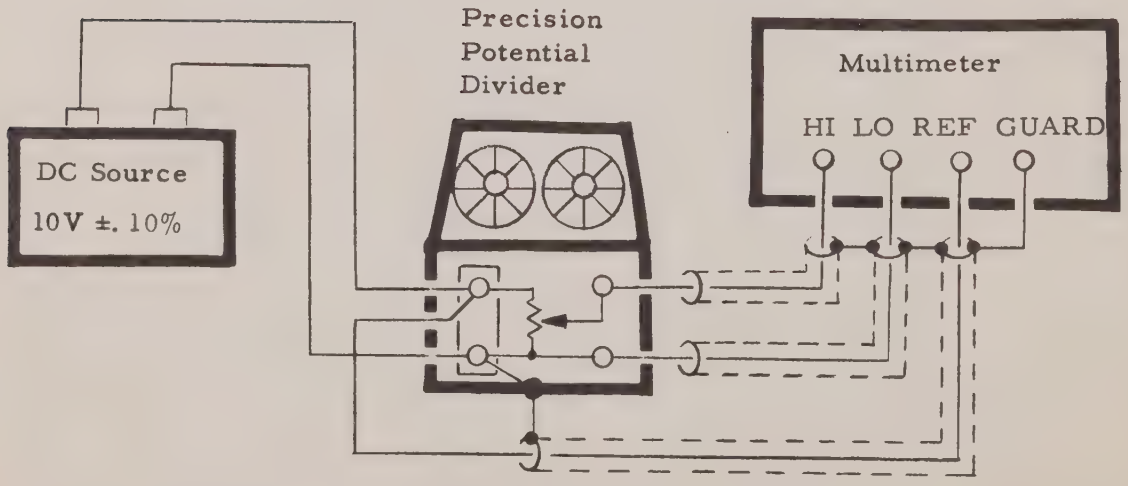


Figure 4.2. Precision Potential Divider Input Connections for Checking DC/DC Ratio Measurements

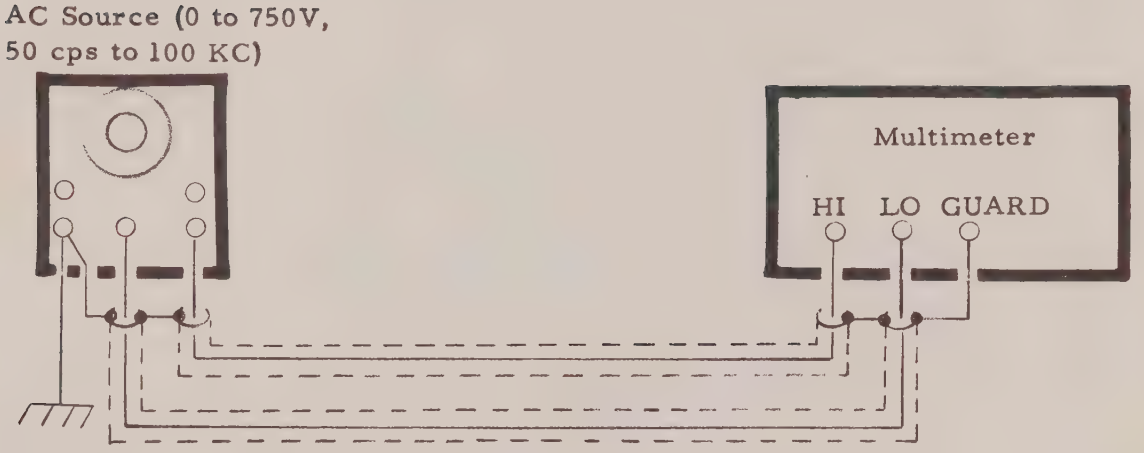


Figure 4.3. Setup for Checking AC Volts Measurements

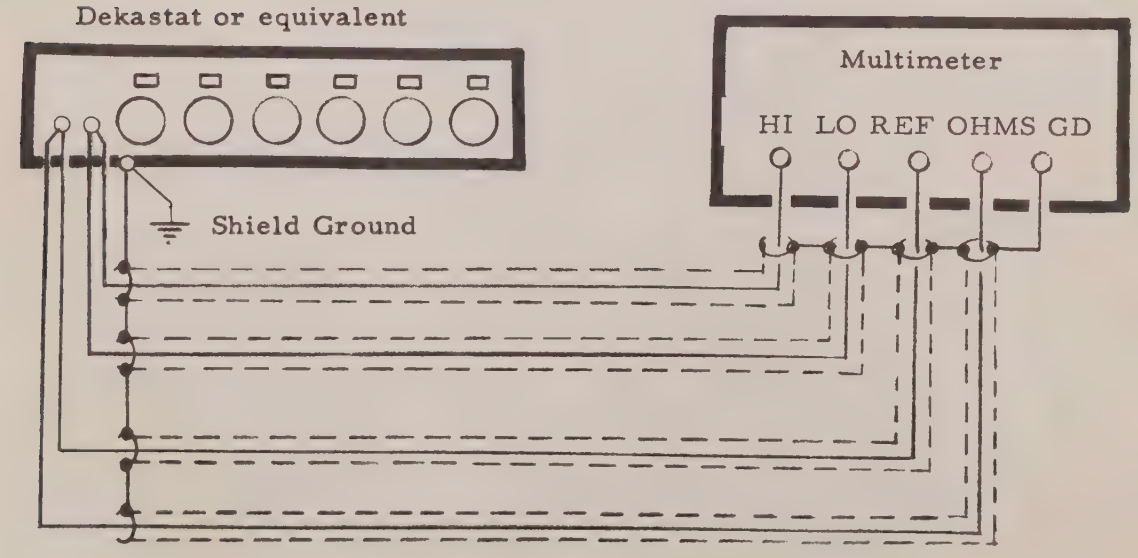


Figure 4.4. Setup for Checking Resistance Measurements

g. Connect a 1.5 volt battery in series with a 60 Hz AC source to the meter input terminals. Set the AC input to 100 microvolts (peak to peak). Use an oscilloscope to determine the exact AC input. The meter reading will become unstable.

h. Set the FILTER switch to IN. The meter reading will become stable.

NOTE

In the "filter-in" mode, the encoding rate is slowed down and time must be allowed between adjustments.

i. Slowly increase the AC input signal until the meter again becomes unstable. The meter should remain stable until the AC input signal exceeds 100 millivolts (zero to peak).

j. Remove the AC source from the meter. Set the FILTER switch to OUT and the RANGE switch to AUTO.

k. If it is desired to check the print level outputs of the meter, connect an external printer to connectors J101 and J102 and perform steps l through 0. If not, proceed with step p.

l. Set the instrument front panel switches as follows:

POWER	ON
ENCODE	SINGLE
MODE	DC
RANGE	10V
FILTER	OUT

m. Apply .00000V to the instrument. Set the ENCODE switch to the spring loaded position and release. The printer will record the measurement.

n. Increase the input voltage 1 digit at a time and activate the ENCODE switch for each step. The voltage should be increased in appropriate integers to check all digits in all decades.

o. Set the MODE switch successively to all positions, and activate the ENCODE switch for each position. Observe that the correct symbol is recorded on the printed format.

p. Set the ENCODE switch to CONT and the MODE switch to DC. Disconnect the signal input clips from the signal input and short them together. The front panel display should be stable and read ±.00000 ± 1 digit.

q. Set the MODE switch to RATIO.

r. Connect the signal input cable for ratio measurements as illustrated in Figure 4.2.

s. Adjust the precision potential divider for an output between 1 and 10 volts. The meter will display the correct ratio and the letter R.

t. Remove the signal input and set the MODE switch to AC.

u. Connect the signal input cable for AC measurements as illustrated in Figure 4.3.

v. Adjust the AC source for a 100 Hz output between 0 and 1 volt, 1 and 10 volts, 10 and 100 volts, and then between 100 and 750 volts. The meter will range automatically to the correct range and display the correct voltages and the ~ symbol.

w. Repeat step v, this time setting the RANGE switch to 1V and then to successively higher range positions. Note that the meter reads the voltages in the correct ranges.

x. Set the RANGE switch to the AUTO position.

y. Remove the signal input and set the MODE switch to OHMS.

CAUTION

Do not connect the GUARD terminal to any of the four input leads: HI, LO, OHMS or REF.

z. Short the OHMS and REF terminals together. Also short the HI and LO terminals together, but do not allow the two pairs of jumpered leads to come in contact with each other or with the GUARD. The readout should now indicate 9999.9K.

aa. Connect the meter to a precision resistance source as illustrated in Figure 4.4. The readout should indicate the value of the resistance selected, within the specified tolerance. The decimal point should be properly positioned according to the range of the external resistance.

bb. Set the RANGE switch to each of the ohms range positions and observe that the decimal point changes positions accordingly.

NOTE

This procedure should be done slowly since a delay is necessary for the meter to encode in each range.

4.2 CALIBRATION PROCEDURE (DC and Ratio)

Calibration adjustments and test points are illustrated in Figure 4.5. All adjustments are accessible at the front of the meter.

4.2.1 Test Equipment Required

DC voltage standards should be compared with a group of saturated standard cells which have been certified by the National Bureau of Standards. Test equipment is listed below:

a. DC Voltage Standard , variable between 0 and 1000 volts, adjustable in steps of 1 microvolt: Kintel Model 303 or equivalent.

b. Precision 10 volt DC source.

c. Precision Potential Divider: Dekavider or equivalent.

4.2.2 Absolute Calibration

a. Set instrument front panel switches as follows:

POWER	ON
ENCODE	CONT
MODE	DC
RANGE	10V
FILTER	OUT

b. Short HI and LO input leads and GUARD together. Meter should read + or - 0.0000V. If this is not the case, adjust instrument to zero using absolute zero adjustment, R73 on board 16.

c. Apply -9.9855V to the instrument using the precision DC source.

d. Adjust R65 on board 16 for a meter reading of -9.9855V.

e. Reverse input leads to the instrument at the precision DC source.

f. Adjust R79 on board 16 for a meter reading of +9.9855V.

4.2.3 Preamplifier Adjustments (1V Range)

a. Set front panel switches as follows:

POWER	ON
ENCODE	CONT
MODE	DC
RANGE	1V
FILTER	IN or OUT (Filter automatically selected in this range).

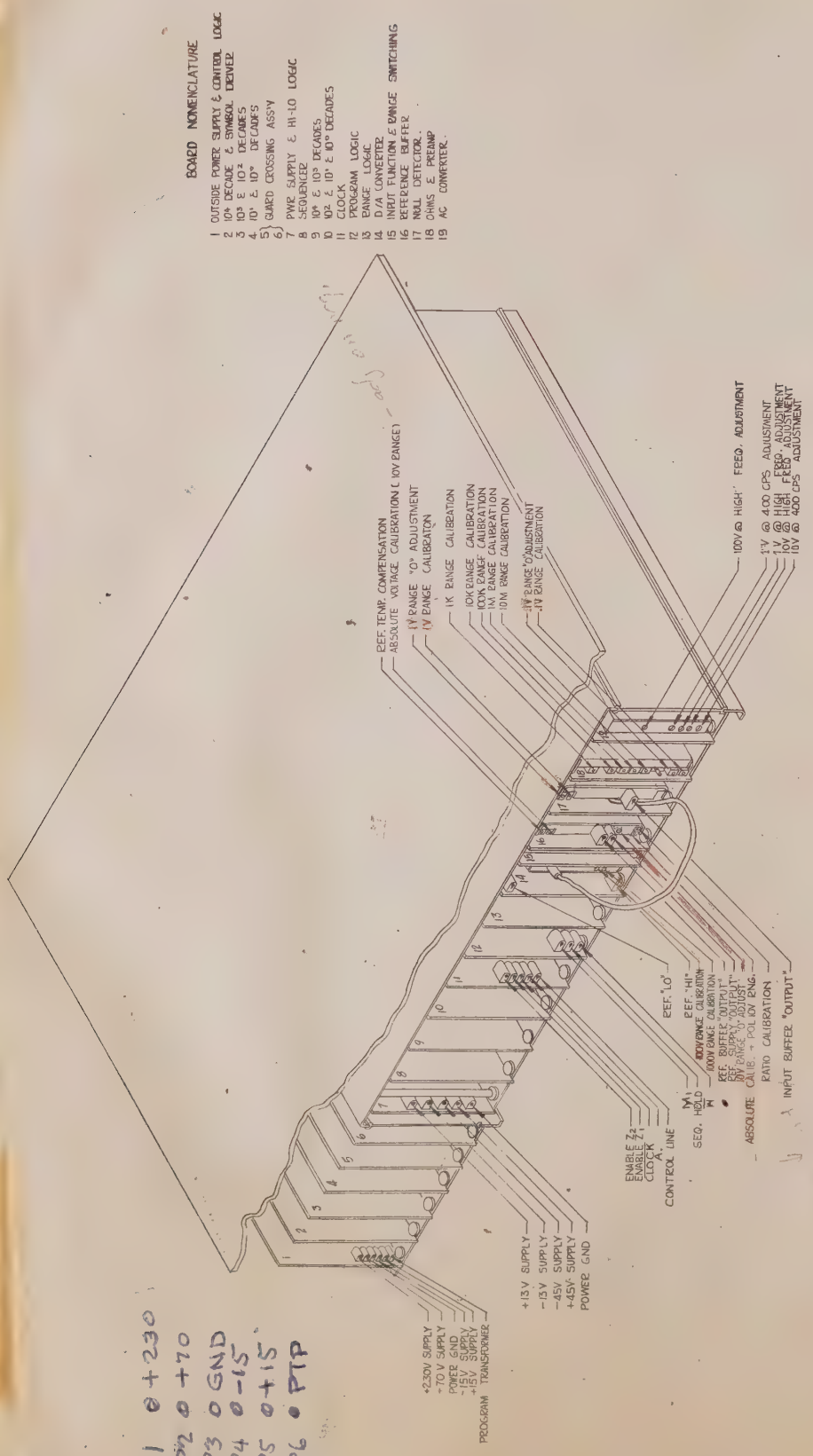


Figure 4.5. Location of Test Points and Calibration Adjustments

b. Short HI and LO input leads and GUARD together. Meter should read + or - .00000V. If this is not the case, adjust the zero adjustment for the 1V range, R145 on board 17, until the meter reads .00000V.

c. Apply +.99855V to the instrument using precision DC source.

d. Adjust R109 on board 17 for a meter reading of +.99855V.

e. Reverse the input leads to the instrument at the precision DC source.

f. The instrument should read -.99855V ±2 digits. If this is not the case, readjust the zero adjustment as in step b above.

NOTE

Some precision DC voltage sources exhibit a low frequency rumble which would cause the instrument to appear unstable. Since the filter would not be able to remove this low frequency interference, it might be necessary to set the DC standard to a voltage of ±9.9855V and use a precision voltage divider to divide this voltage by 10.

4.2.4 Preamplifier Adjustment (.1V Range)

NOTE

The following procedure is required only when the preamplifier accessory is installed in the instrument.

a. Set front panel switches as follows:

POWER	ON
ENCODE	CONT
MODE	DC
RANGE	.1V
FILTER	IN or OUT (filter automatically selected in this range)

b. Short HI and LO input leads and GUARD together. Meter should read + or - 00.000MV. If this is not the case adjust zero adjustment for .1V range, R14 on board 18, until the meter reads + or - 00.000 MV.

c. Apply +99.855 MV to the instrument using precision DC source.

d. Adjust R8 on board 18 for a meter reading of +99.855 MV.

e. Reverse input leads to the instrument at the precision DC source.

f. The instrument should read -99.855 MV ±5 digits. If this is not the case, readjust the zero adjustment as in step b above.

NOTE

If the precision DC voltage source has a low frequency rumble, it may be necessary to set the DC standard to a voltage of ±9.9855V and use a precision voltage divider to divide this voltage by 100.

4.2.5 Input Attenuator Adjustments

WARNING

High and potentially dangerous DC voltages are used in calibrating the 100V and 1000V ranges. Therefore, the DC standard output should be reduced or turned off when connecting the meter inputs to the voltage standard.

a. Set RANGE switch to 100V.

b. Apply 99.985 volts to the instrument.

c. Adjust R90 on board 15 until the instrument reads 99.985 volts.

d. Set RANGE switch to 1000V.

e. Apply 999.85 volts to the instrument.

f. Adjust R92 on board 15 until instrument reads 999.85 volts.

4.2.6 Ratio Calibration

Ratio calibration of the instrument consists of calibrating the lowest ratio range (ratio of 1).

a. Set instrument front panel switches as follows:

POWER	ON (If instrument has been on uninterrupted for at least 15 minutes, no warmup time is required. If not, warm up for 15 minutes).
ENCODE	CONT
MODE	RATIO
RANGE	1
FILTER	OUT

b. Connect instrument input terminals as shown in Figure 4.2.

c. Set Dekavider to 99855.

d. The instrument should read R. 99855. If this is not the case, adjust R77 on board 16 until the meter reads R. 99855.

e. Reverse the output polarity of the precision DC source. The meter should indicate the same reading + or - 2 digits.

4.2.7 Linearity Check and Calibration of Bridge

The linearity check of the instrument bridge is best performed in the ratio mode. Calibration of the bridge is not normally required. The resistors making up the bridge are fixed precision resistors and are doubly aged. Resistor failure rarely occurs. If one of these resistors should change value, it must be replaced as outlined in section V, paragraph

a. Set instrument front panel switches (with the exception of the RANGE switch) as in paragraph 4.2.6.

b. Connect the instrument to the potential divider and the calibration source as illustrated in Figure 4.2.

c. Turn all potential divider dials to 0 and short the output leads together. The instrument should read R. 00000.

d. Remove the short from the potential divider and raise the voltage of the signal input to the meter in increments sufficient to increase the ratio reading one digit at a time. Begin with the units decade to check if all digital values are included. Transfer points are listed in Table 4.1.

4.3 CALIBRATION PROCEDURE (AC)

The calibration of the AC converter should be performed only after DC calibration is completed. AC calibration is divided into two sections:

Table 4.1. Transfer Points

00000 to 00001	00069 to 00070	03999 to 04000
00001 to 00002	00079 to 00080	04999 to 05000
00002 to 00003	00089 to 00090	05999 to 06000
00003 to 00004	00099 to 00100	06999 to 07000
00004 to 00005	00199 to 00200	07999 to 08000
00005 to 00006	00299 to 00300	08999 to 09000
00006 to 00007	00399 to 00400	09999 to 10000
00007 to 00008	00499 to 00500	19999 to 20000
00008 to 00009	00599 to 00600	29999 to 30000
00009 to 00010	00699 to 00700	39999 to 40000
00019 to 00020	00799 to 00800	49999 to 50000
00029 to 00030	00899 to 00900	59999 to 60000
00039 to 00040	00999 to 01000	69999 to 70000
00049 to 00050	01999 to 02000	79999 to 80000
00059 to 00060	02999 to 03000	89999 to 90000

zero adjustments and AC range adjustments. Adjustment and test point locations are illustrated in Figure 4.6. The adjustments must be performed in the order listed in the calibration procedure.

Zero adjustments are outlined in paragraph 4.3.2. The first four steps (a through d) ascertain whether this procedure need be carried any further. If it is necessary to perform the zero adjustments, a board extender is required. Board Extender, Part No. 105-124-84, should be ordered from Honeywell Inc. The extender board plugs into the AC converter board connector and occupies the position normally occupied by the circuit board. The AC converter board is then connected to the extender, exposing both the circuitry and component sides for calibration or troubleshooting.

NOTE

When using the board extender, connect board extender shield to T. P. 5, board 7.

The AC range adjustments are outlined in paragraph 4.3.3. For this procedure, an Optimation Model AC104A Power Source and a thermal transfer voltmeter are required, as listed in paragraph 4.3.1. If a Model AC104A Power Source is not available, a Holt Model 323A (or equivalent) can be used for calibration at 400 Hz only. If the Holt Model 323A is used, it must be calibrated to 0.02%; otherwise it should be used with the thermal transfer voltmeter.

When the thermal transfer voltmeter is used, consult the manual included with the instrument for operating instructions. Block diagram Figure 4.7 shows a typical calibration setup using a thermal transfer voltmeter and is given only as a guide in use of this type of equipment.

NOTE

The board extender should not be used for AC range adjustments.

4.3.1 Equipment Required

a. Extender Board, Part No. 105-124-84.

b. Optimation Model AC104A AC Power Source, 50 Hz to 100 KHz, 0 to 500V RMS (Optimation Inc., 7243 Atoll Avenue, North Hollywood, California).

c. Holt Model 62 Thermal Transfer Voltmeter or equivalent.

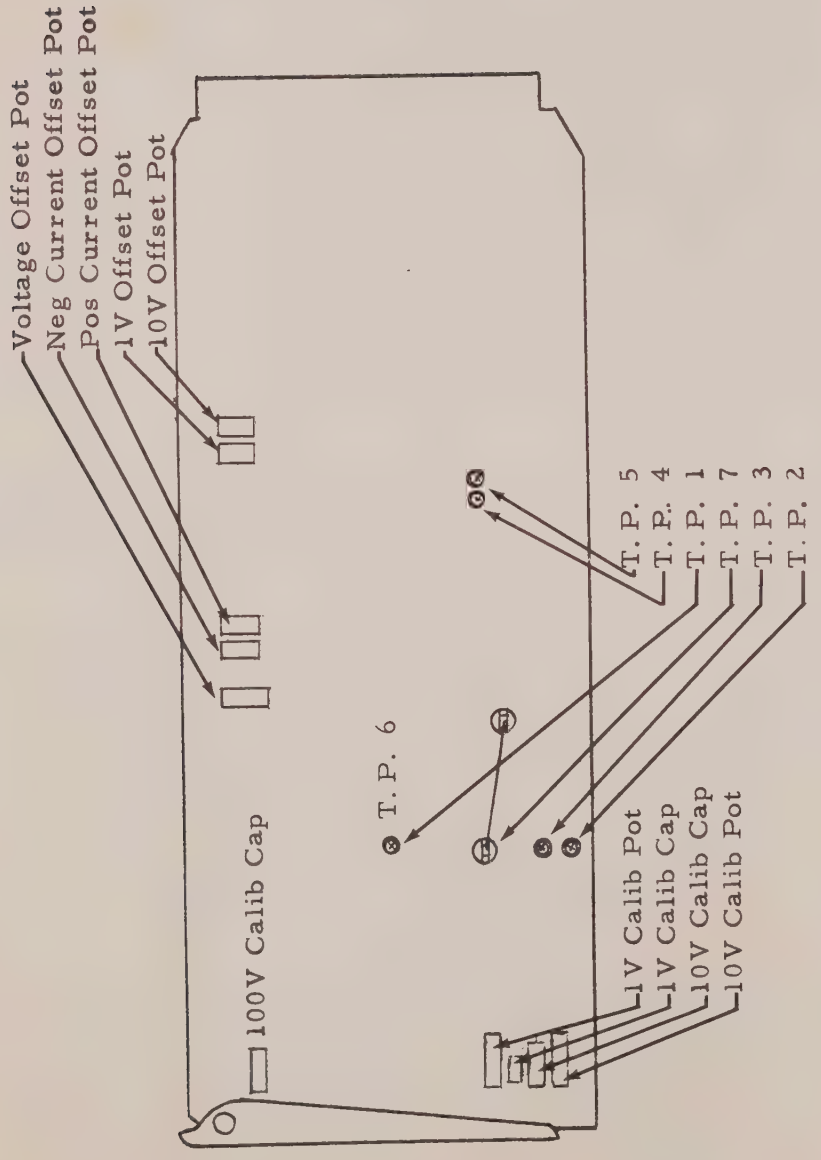


Figure 4.6. Location of AC Converter Adjustments and Test Points (Board 19)

d. DC Voltage Standard with 4-wire capability, accurate to ±0.01%, Kintel Model 321 or equivalent.

NOTE

A DC standard without 4-wire capability can be used, if the Model EI-85 is used as a monitoring device. To monitor the DC voltage, connect the Model EI-85 to the DC standard output at the points of connection with the thermal transfer voltmeter, and set the EI-85 for DC mode and appropriate range. It will then be necessary to switch the lead connections from the EI-85 back and forth between the DC and AC terminal connections on the transfer voltmeter during the AC range adjustments.

e. DC voltmeter with resolution of approximately 10 microvolts (may substitute a 100 μV/cm DC oscilloscope such as a Tektronix Model 502A).

WARNING

High and potentially dangerous voltages can be delivered by the type of AC voltage standard used in this calibration procedure. Therefore, the AC voltage output should be reduced or turned off when connecting signal input leads to the AC voltage standard.

4.3.2 Zero Adjustments

a. Set the Model EI-85 front panel switches as follows:

POWER	ON (Allow fifteen minutes warmup)
ENCODE	CONT
MODE	AC
RANGE	1V
FILTER	IN or OUT (filter is automatically selected in this mode)

b. Short HI and LO input leads and GUARD together. Meter should read 3 digits or less in the least significant decade.

c. Set RANGE switch to 10V. Meter should read 2 digits or less.

d. Set the RANGE switch to 100V. Meter should read 3 digits or less. If the meter has responded properly to this point, it will not be necessary to perform the rest of this procedure. Refer to paragraph 4.3.3. If the meter has displayed an offset greater than that specified above, perform the steps below.

e. Turn the POWER switch to OFF. Remove the AC converter board from the instrument and reconnect with board extender. Connect board extender shield to T.P. 5, board 7. Turn the POWER switch to ON. Measure the voltage at T.P. 6 (see Figure 4.6) with the DC Voltmeter. The voltage should be between +0.8V and +1.2V. If this is not the case, refer to section V of this manual for trouble shooting techniques.

f. Set RANGE switch to 10V.

g. Short T.P. 1 (Figure 4.6) to the AC converter board shield.

h. Short T.P. 2 to T.P. 7.

i. Measure the voltage at T.P. 3 with the DC voltmeter. Adjust the voltage offset potentiometer (Figure 4.6) for a reading of 0V ±10μV on the DC Voltmeter.

j. Disconnect T.P. 2 and T.P. 7 and set the RANGE switch to 1V.

k. Adjust the negative offset potentiometer (Figure 4.6) for a reading of 0V ±20μV on the DC Voltmeter.

l. Disconnect T.P. 1 from the shield.

m. Adjust the positive current offest potentiometer (Figure 4.6) for a reading of 0V ±20μV on the DC voltmeter.

n. Disconnect the DC voltmeter from Tp+p 3.

o. Adjust the 1V Offset potentiometer for a meter reading of ~.00000V (front panel of Model EI-85).

p. Set the RANGE switch to 10V.

q. Turn the POWER switch to OFF. Disconnect board extender and re-insert AC converter board into instrument. Turn the POWER switch to ON.

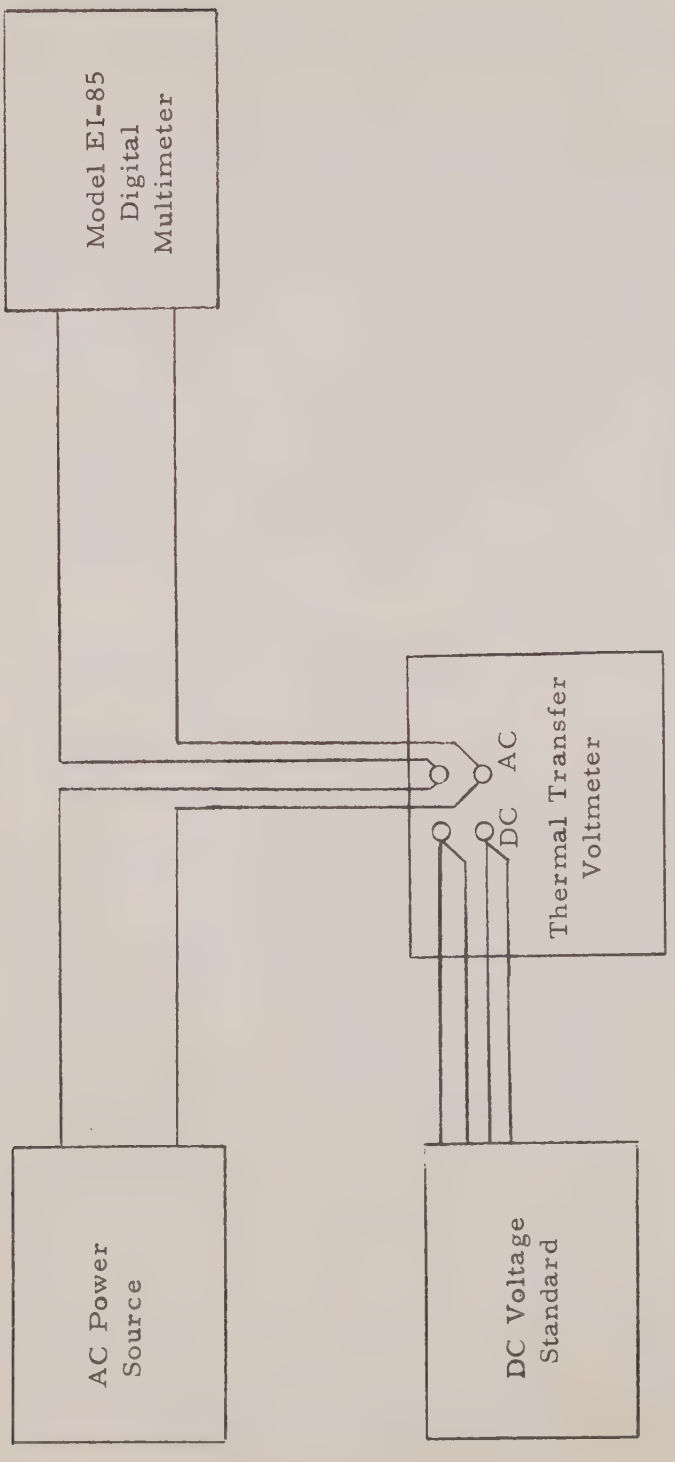


Figure 4.7. Typical Setup Using Thermal Transfer Voltmeter for AC Calibration

4.3.3 AC Range Adjustments

a. Connect the test equipment as illustrated in Figure 4.7.

b. Set the Model EI-85 front panel controls as follows:

POWER	ON (Allow fifteen minutes warmup)
ENCODE	CONT
MODE	AC
RANGE	1V
FILTER	IN or OUT

c. Set the DC voltage standard to .98000V and calibrate the thermal transfer voltmeter (refer to instruction manual included with thermal transfer voltmeter).

d. Adjust the AC power source for an output of .98000V AC at 400 Hz. (Use 16V tap on Optimation Model AC104A AC Power Source).

NOTE

Each time the AC power source output is changed, either in voltage or frequency, it will be necessary to recalibrate the thermal transfer voltmeter. Also, it will be necessary to continuously monitor the thermal transfer voltmeter when calibrating the Model EI-85, since AC drift could occur during the short intervals between the steps of this procedure.

e. Adjust the 1V potentiometer (Figure 4.6) for a meter reading of .98000V.

f. Adjust the AC power source for an output of .98000V at 80 KHz.

g. Adjust the 1V capacitor (Figure 4.6) for a meter reading of .98000V.

h. Set the RANGE switch to 10V.

i. Adjust the AC power source for an output of 9.8000V at 400 Hz. (Use 40V tap on Optimation Model AC104A AC Power Source).

j. Adjust the 10V potentiometer (Figure 4.6) for a meter reading of 9.8000V.

k. Adjust the AC power source for an output of 9.8000V at 80 KHz.

l. Adjust the 10V capacitor (Figure 4.6) for a meter reading of 9.8000V.

m. Adjust the AC power source for an output of 98.000V at 80 KHz. (Use 160V tap on Optimation Model AC104A AC Power Source).

n. Adjust the 100V capacitor (Figure 4.6) for a meter reading of 98.000V.

o. Repeat steps b through n above.

4.4 CALIBRATION PROCEDURE (OHMS)

4.4.1 Test Equipment Required

For the ohms mode calibration, a precision resistance source accurate to .005% of full scale value for each meter range is required. This can be a Dekastat (adjustable in steps of 10 milliohms) or equivalent.

4.4.2 Ohms Calibration

The ohms calibration adjustments are located on the ohms amplifier board 18.

a. Set instrument front panel switches as follows:

POWER	ON (warm up for 15 minutes)
ENCODE	CONT
MODE	OHMS
RANGE	1K
FILTER	IN or OUT (filter automatically selected in this mode)

b. Connect the instrument input terminals to the Dekastat (or equivalent) as illustrated in Figure 4.4.

CAUTION

There should be no external voltage across the test resistance. Also, the GUARD terminal should not be connected to any of the four input leads.

c. Set the Dekastat controls for .99955 kilohms.

d. The instrument should read K. 99955. If not, Adjust R34 on board 18 until the reading is *. 99955.

e. Set the RANGE switch to 10K. Apply 9. 9955 kilohms resistance to the input terminals.

f. The meter should read K9. 9955. If not, adjust R32 on board 18 until the reading is K9. 9955.

g. Set the RANGE switch to 100K. Apply a 99. 955 kilohms resistance to the input terminals.

h. The meter should read K99. 955. If not, adjust R141 on board 18 until the reading is K99. 955.

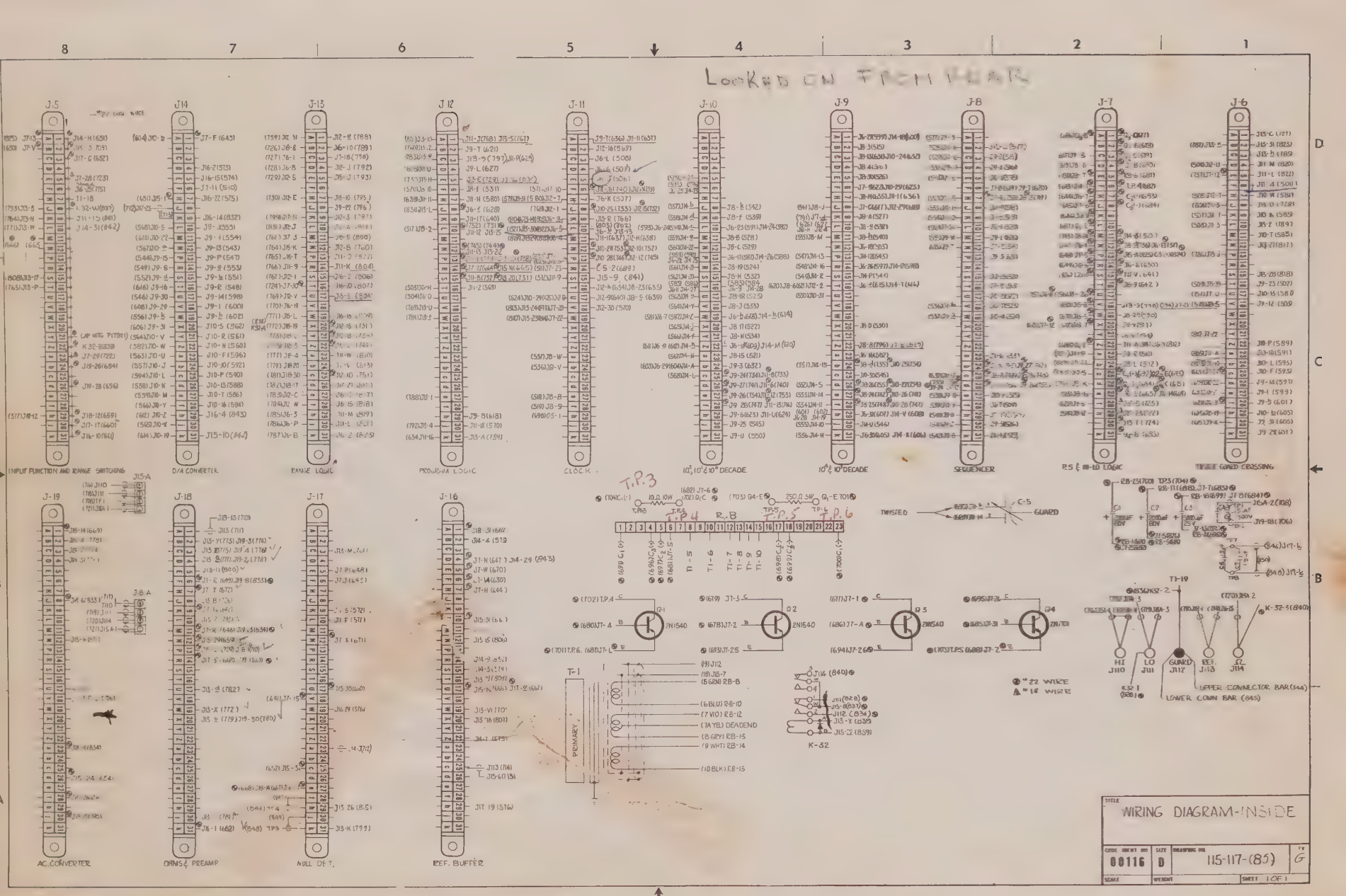
i. Set the RANGE switch to 1M. Apply a 999. 55 kilohms resistance to the input terminals.

j. The meter should read K999. 55. If not, adjust R 37 on board 18 until the reading is K999. 55.

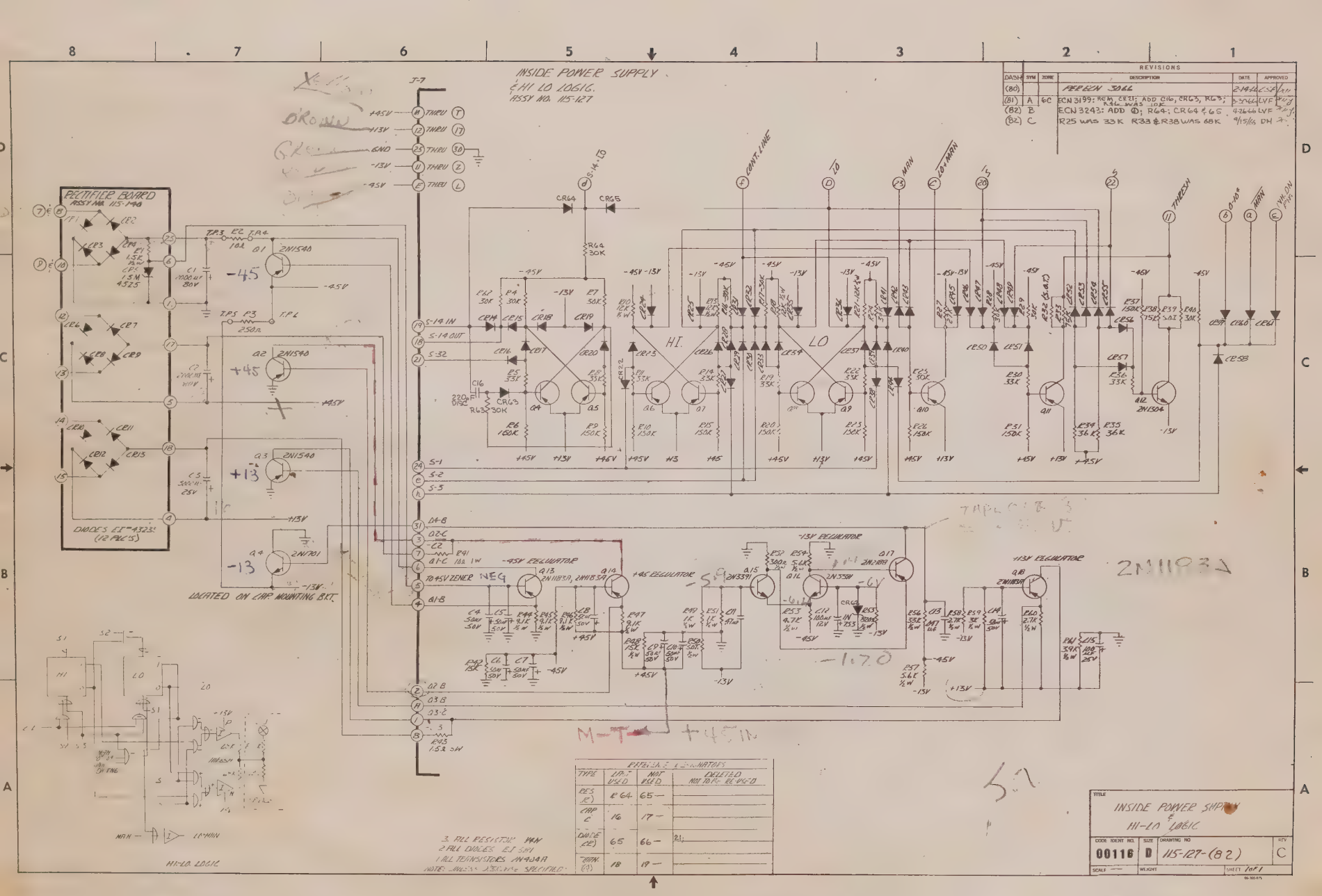
k. Set the RANGE switch to 10M. Apply a 9995. 5 kilohms resistance to the input terminals.

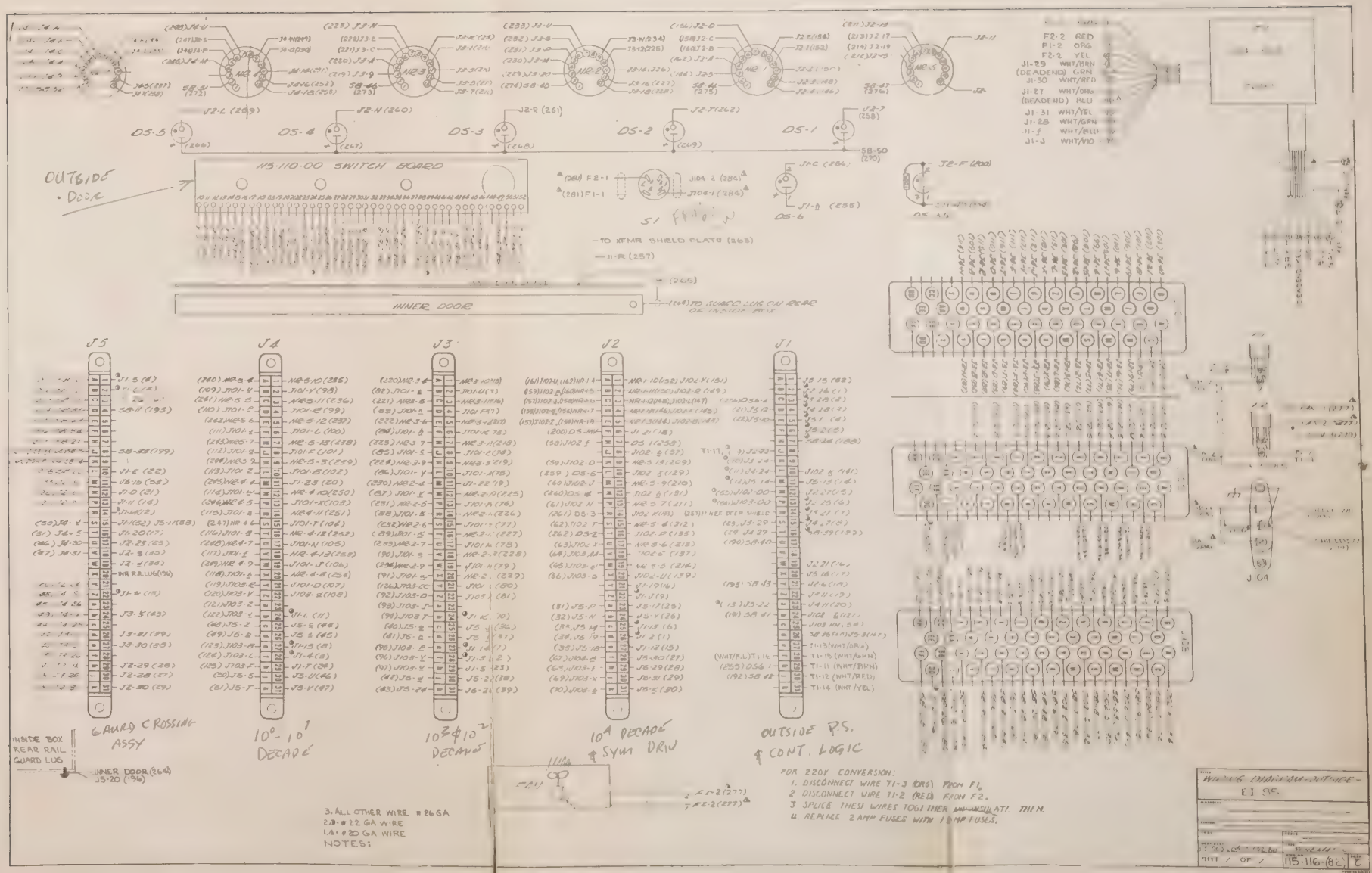
l. The meter should read K99995. 5. If not, adjust R36 on board 18 until the reading is K995. 5.

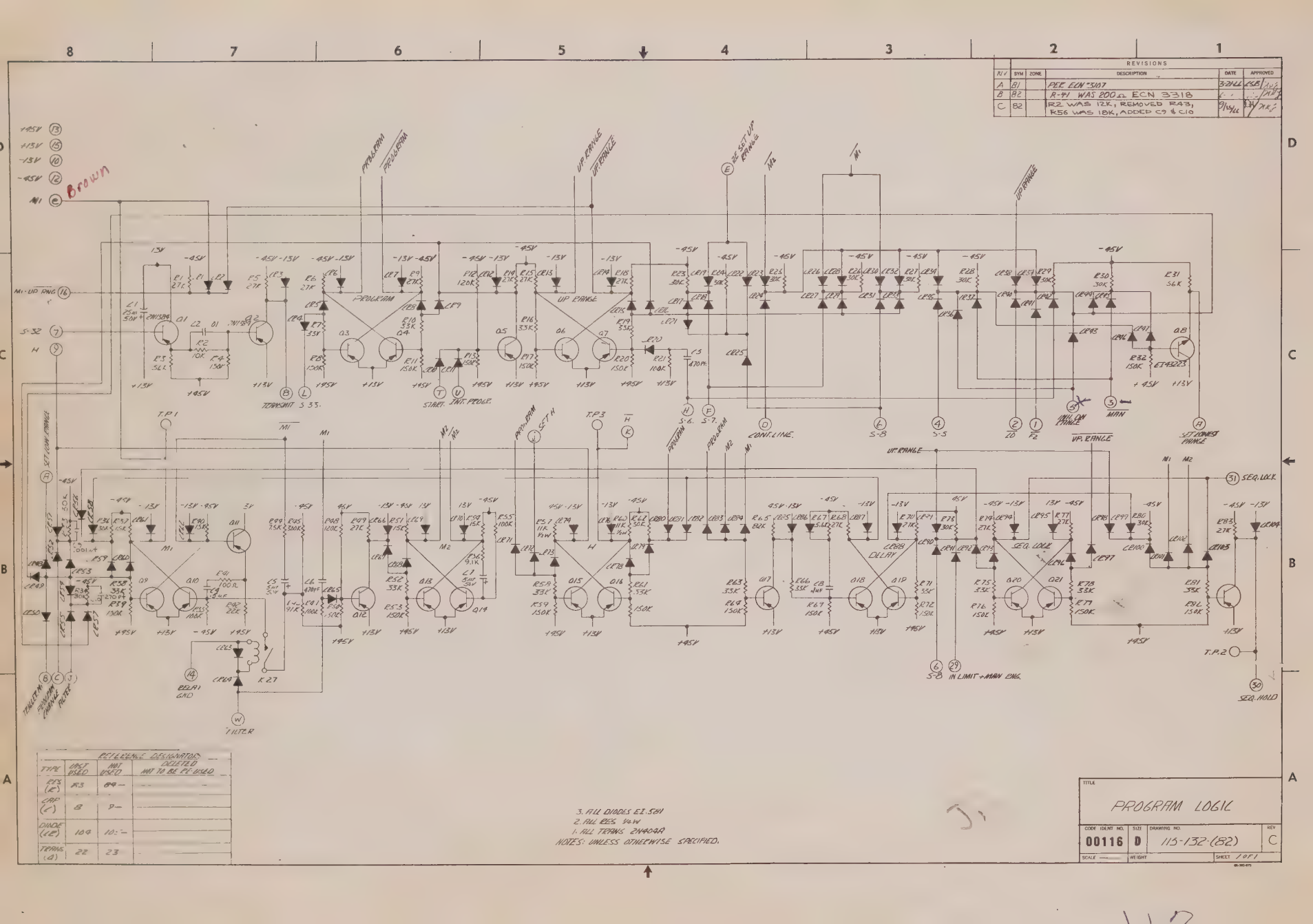
This completes the calibration procedure.


LOOKED ON FROM REAR
J-5
J-14
J-13
J-12
J-11
J-10
J-9
J-8
J-7
J-6
INPUT FUNCTION AND RANGE SWITCHING
D/A CONVERTER
RANGE LOGIC
PROGRAM LOGIC
CLOCK
10⁵, 10⁴ & 10³ DECADE
10² & 10¹ DECADE
SEQUENCER
RS & HI-LO LOGIC
TRIPLE LINED CROSSING
J-19
J-18
J-17
J-16
AC CONVERTER
OHMS & PREAMP
NULL DET.
REF. BUFFER
T.P.3
T.P.4
T.P.5
T.P.6
R.B
TWISTED
GUARD
T-1
PRIMARY
K-32
T-19
HI J110
LO J111
GUARD J112
EXT. J113
EXT. J114
UPPER CONNECTOR BAR (644)
LOWER COMM BAR (645)
"22 WIRE
"16 WIRE
WIRING DIAGRAM-INSIDE
00116
D
115-117-(85)
G
SHEET 1 OF 1

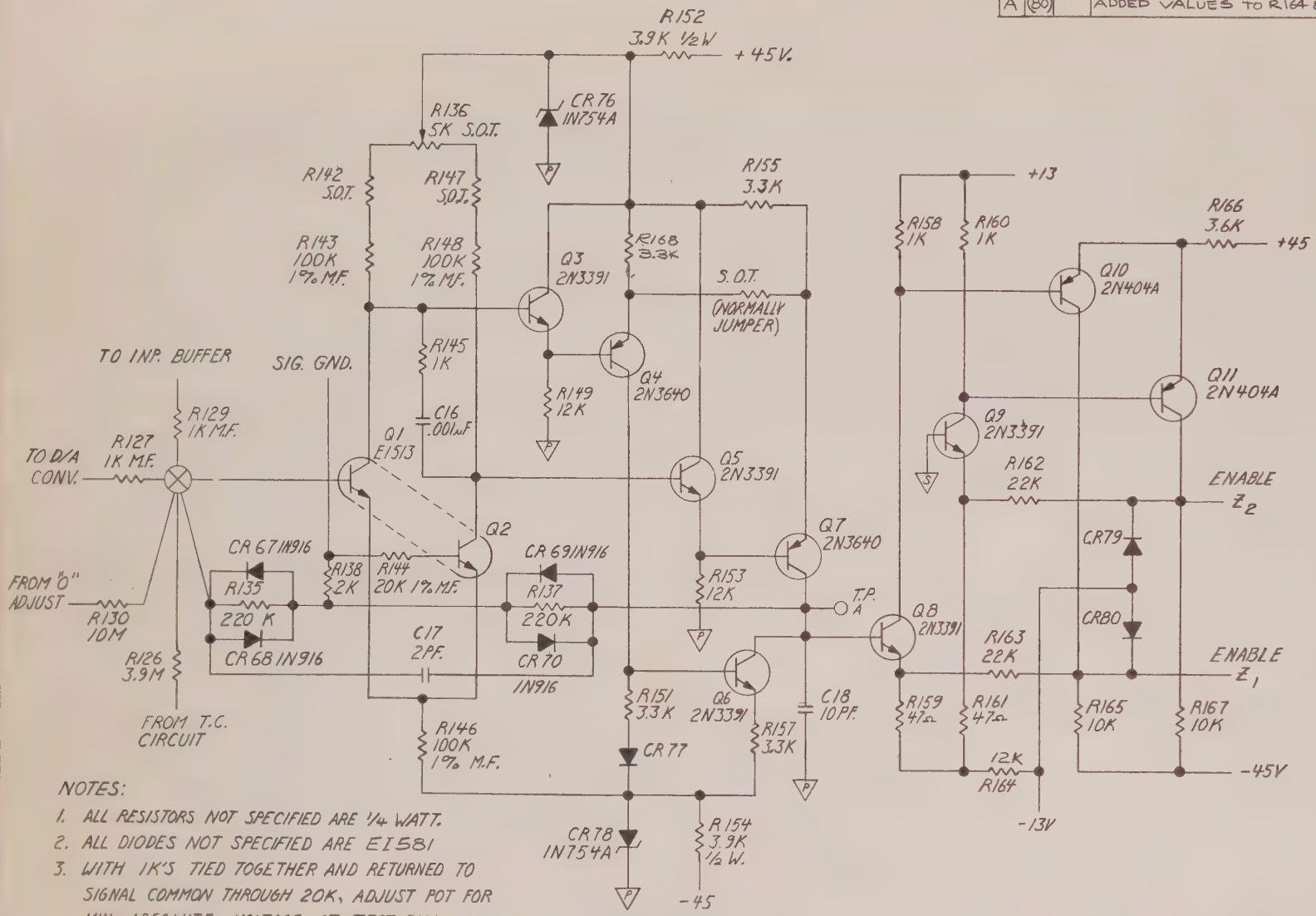



INSIDE POWER SUPPLY
HI LO LOGIC
ASSY NO. 115-127
REVISIONS
DASH | SYM | ZONE | DESCRIPTION | DATE | APPROVED
(80) | | | PER ECN 3066 | 2-14-74 | LC-SA
(81) | A | 6C | ECN 3199: REM. CR21; ADD C16, CR63, R63; R34 WAS 10K | 5-31-74 | LVF
(82) | B | | ECN 3243: ADD D; R64; CR64 & 65 | 4-26-74 | LVF
(82) | C | | R25 WAS 33K R33 & R38 WAS 68K | 9/15/76 | DH
RECTIFIER BOARD ASSY NO. 115-140
DIODES E1 = 4323 (12 PLACES)
LOCATED ON CAP MOUNTING BKT.
+45V ZENER NEG
-45V REGULATOR
+45 REGULATOR
-13V REGULATOR
+13V REGULATOR
CONT. LINE
HI
LO
MAN
LO MAN
THRESH
2N1893
2N3391
2N3638
2N1504
2N1701
2N1540
2N1541A
3 FILL RESISTOR MAN
2 FILL DIODES E1 S&V
1 FILL TRANSISTORS 2N404A
NOTE: UNLESS OTHERWISE SPECIFIED
RESISTOR ELIMINATORS
TYPE | NO. USED | NOT USED | DELETED NOT TO BE RE-USED
RES (R) | R 64 | 65 — |
CAP C | 16 | 17 — |
DIODE (CR) | 65 | 66 — | 21
TRANS. (Q) | 18 | 19 — |
INTERNAL P. SUPPLY J-7
TITLE: INSIDE POWER SUPPLY HI-LO LOGIC
CODE IDENT NO. 00116 | SIZE D | DRAWING NO 115-127-(82) | REV C
SCALE — | WEIGHT | SHEET 1 of 1


115-110-00 SWITCH BOARD
OUTSIDE DOOR
INNER DOOR
TO XFMR SHIELD PLATE (263)
J1-R (257)
J1-A (256)
J2-F (200)
J5
J4
J3
J2
J1
J104
GUARD CROSSING ASSY
10°-10¹ DECADE
10² ϕ 10³ DECADE
10⁴ DECADE & SYNC DRIV
OUTSIDE P.S. & CONT. LOGIC
INSIDE BOX REAR RAIL GUARD LUG
INNER DOOR (264) J5-20 (196)
FAN
FOR 220V CONVERSION:
1. DISCONNECT WIRE T1-3 (ORG) FROM F1.
2 DISCONNECT WIRE T1-2 (RED) FROM F2.
3 SPLICE THESE WIRES TOGETHER AND INSULATE THEM.
4. REPLACE 2 AMP FUSES WITH 1 AMP FUSES.
3. ALL OTHER WIRE #26GA
2.B-#22 GA WIRE
1.A-#20 GA WIRE
NOTES:
WIRING DIAGRAM-OUTSIDE-EI 85.
115-116-(82)
SHT 1 OF 1


REVISIONS
REV | SYM | ZONE | DESCRIPTION | DATE | APPROVED
A | B1 | | PER ECN 3307 | 3-24-66 | CSB
B | B2 | | R-71 WAS 200Ω ECN 3318 | 6-1-66 | CSB
C | B2 | | R2 WAS 12K, REMOVED R43, R56 WAS 18K, ADDED C9 & C10 | 9/14/66 | CSB
+45V
+13V
-13V
-45V
N1
Brown
M1-UP RNG
S-32
H
PROGRAM
UP RANGE
TRANSMIT S 33.
START
INIT. PROG.
T.P.1
T.P.3
SET UP LOW RANGE
SET UP HIGH RANGE
CONT. LINE.
S-6
S-7
S-8
S-5
Z0
F2
LOW RANGE
MAN
SEQ. LOCK
SEQ. HOLD
T.P.2
IN LIMIT + MAN ENG.
TRIGGER
PROGRAM CONTROL
FILTER
RELAY GND
K 27
DELAY
SEQ. LOCK
REFERENCE DESIGNATOR
TYPE | USED | NOT USED | DELETED NOT TO BE RE-USED
RES (R) | R3 | R9 — | —
CAP (C) | 8 | 9 — | —
DIODE (CR) | 109 | 110 — | —
TRANS. (Q) | 22 | 23 | —
3. ALL DIODES ED 5811
2. ALL RES. ¼W
1. ALL TRANS 2N404A
NOTES: UNLESS OTHERWISE SPECIFIED.
TITLE
PROGRAM LOGIC
CODE IDENT. NO. 00116
SIZE D
DRAWING NO. 115-132-(B2)
REV C
SCALE
WEIGHT
SHEET 1 OF 1

REVISIONS				
REV	SYM	ZONE	DESCRIPTION	APPROVED
A	(80)		ADDED VALUES TO R164 & R168	12/9/16 DH/JKH

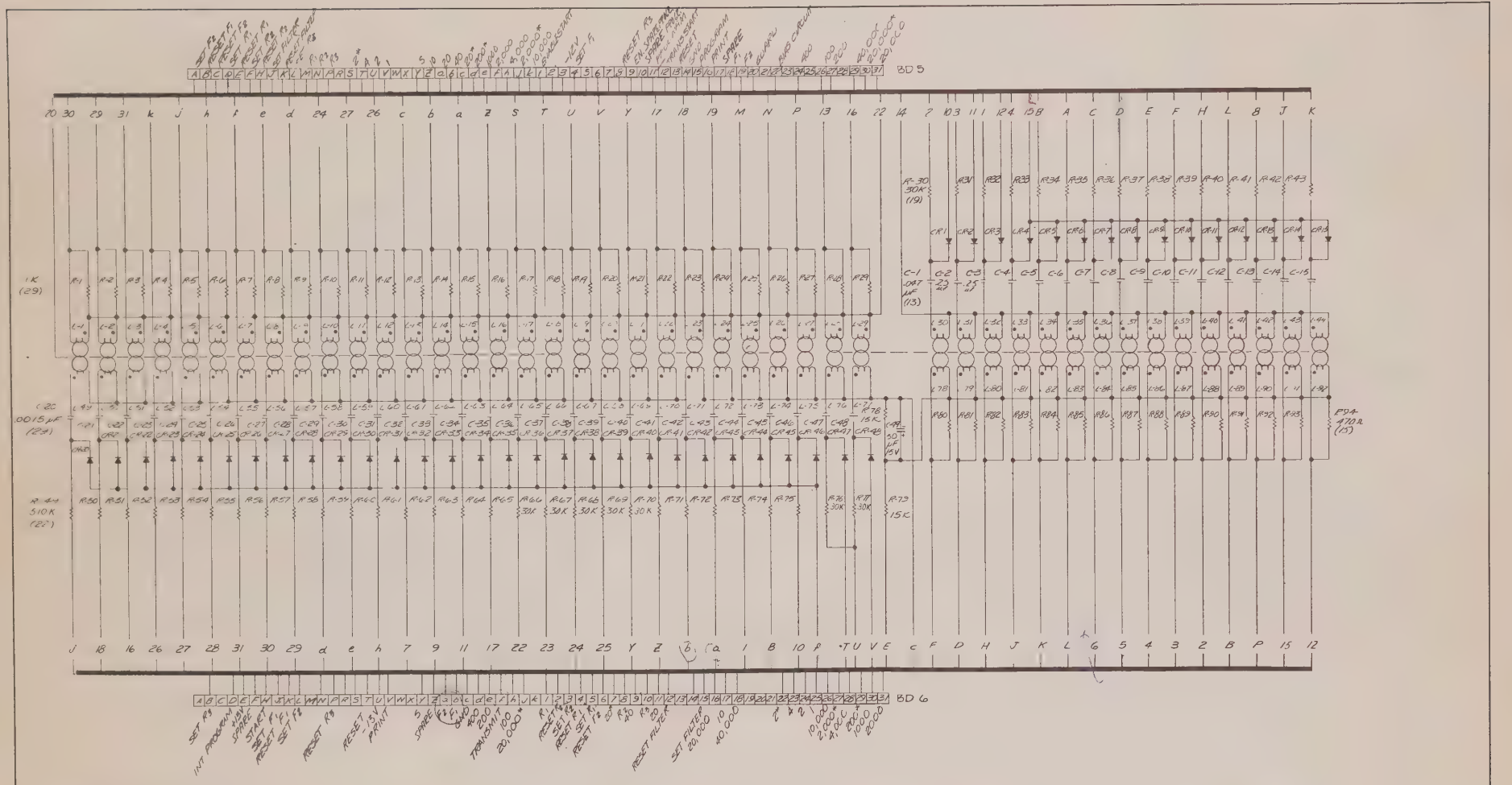


NOTES:

1. ALL RESISTORS NOT SPECIFIED ARE 1/4 WATT.
2. ALL DIODES NOT SPECIFIED ARE E1581
3. WITH 1K'S TIED TOGETHER AND RETURNED TO SIGNAL COMMON THROUGH 20K, ADJUST POT FOR MIN. ABSOLUTE VOLTAGE AT TEST PIN.

TITLE
NULL DETECTOR E185
PART OF ANALOG SECTION

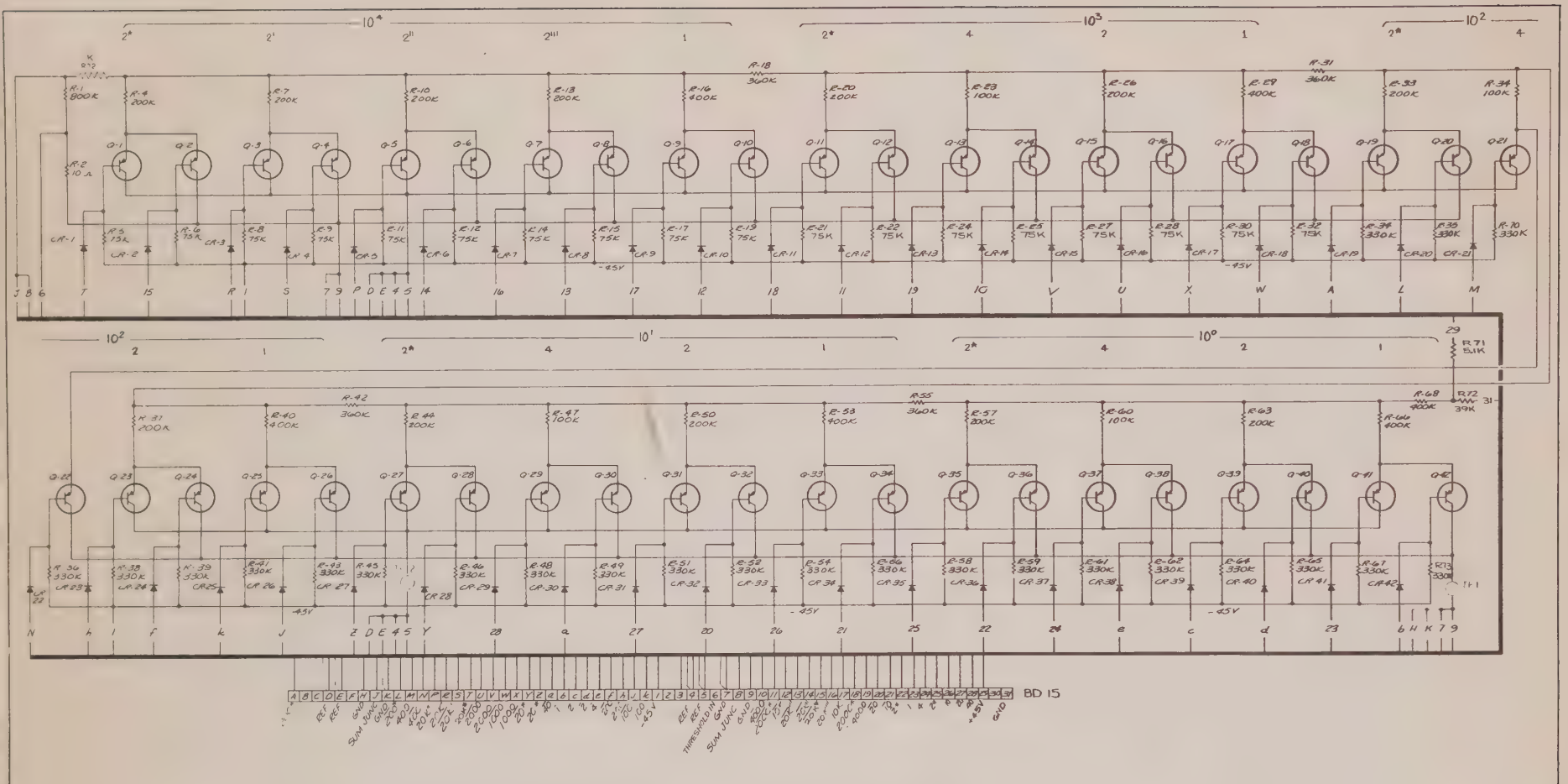
CODE IDENT NO.	SIZE	DRAWING NO.	REV
00116	C	115-137-(80)	A
SCALE NONE	WEIGHT —	SHEET 1 OF 1	



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIODES EI. 581
2. ALL RESISTORS ¼ W

TITLE	GUARD-CROSSING ASS'Y EI 85
MATERIAL	
FINISH	
TOOL	SCALE NONE
NEXT ASSY.	TYPE SCHEMATIC
SHT. 1 OF 1	DWG. NO. 115-120 REV. (80)



NOTES: UNLESS OTHERWISE SPECIFIED
1 ALL TRANSISTORS 2N2374
2 ALL DIODES EI 681

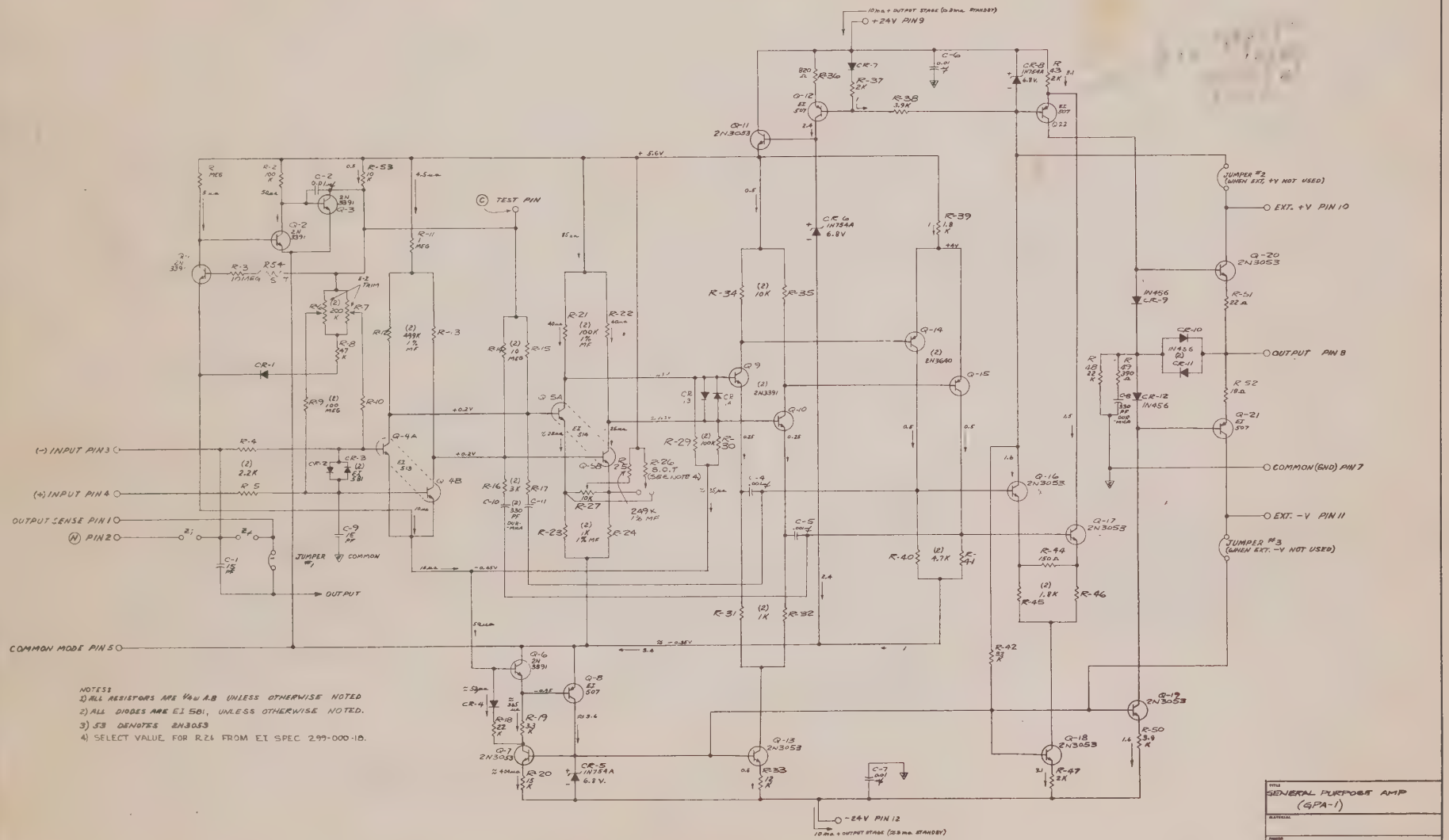
A (80) ADDED VALUE TO R73

BRIDGE
EI 85

BD # 115-134-81

SCHEM

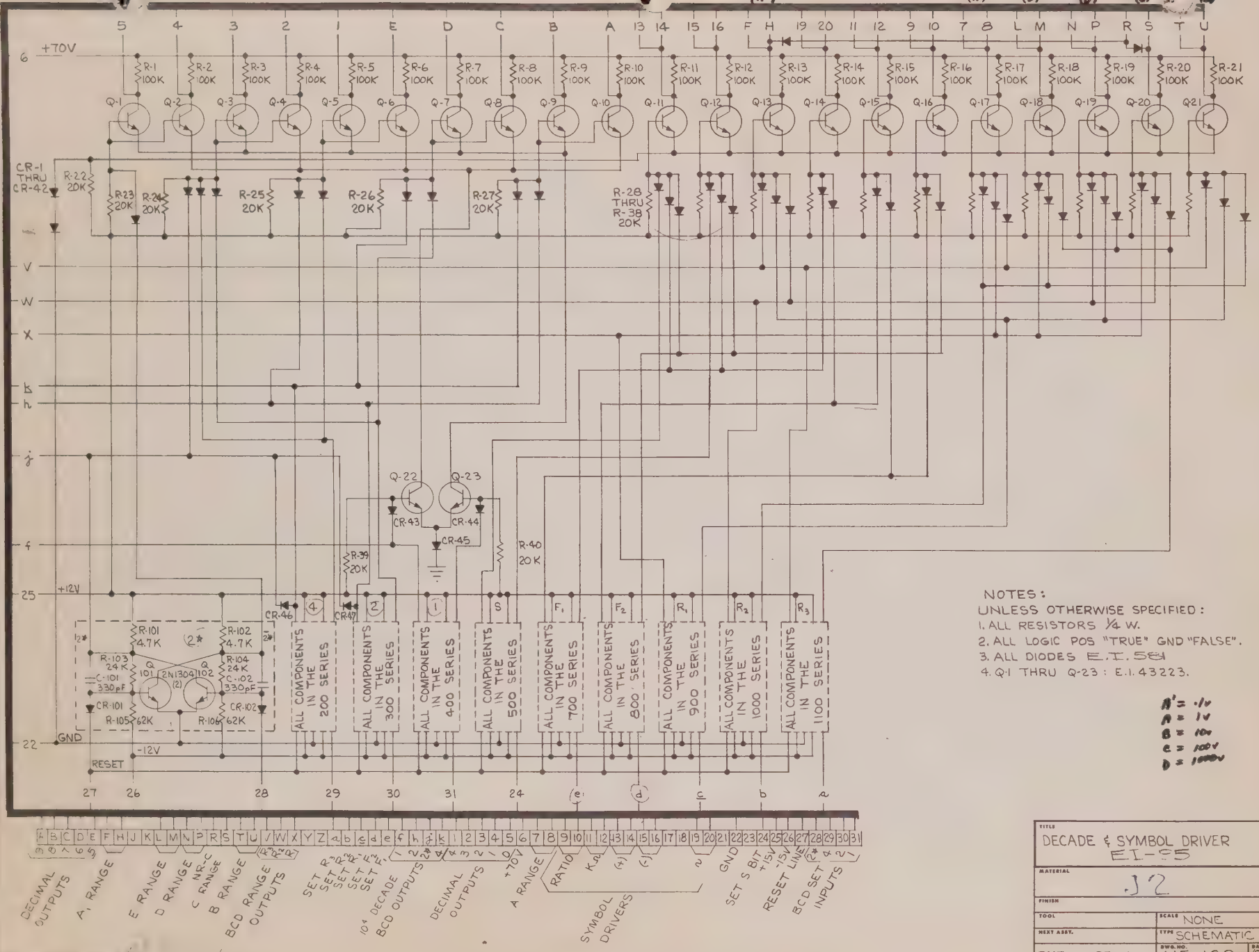
1 1 115-134 (80)



NOTES:
1) ALL RESISTORS ARE ¼W A.B UNLESS OTHERWISE NOTED.
2) ALL DIODES ARE EI 581, UNLESS OTHERWISE NOTED.
3) 53 DENOTES 2N3053
4) SELECT VALUE FOR R.26 FROM EI SPEC 2.99-000-18.

TITLE	GENERAL PURPOSE AMP (GPA-1)
MATERIAL	
FINISH	
TOOL	SCALE
SHEET & SHT.	SCHEM.
SHT. 1 OF 1	501-100 (B1)

GPA-1

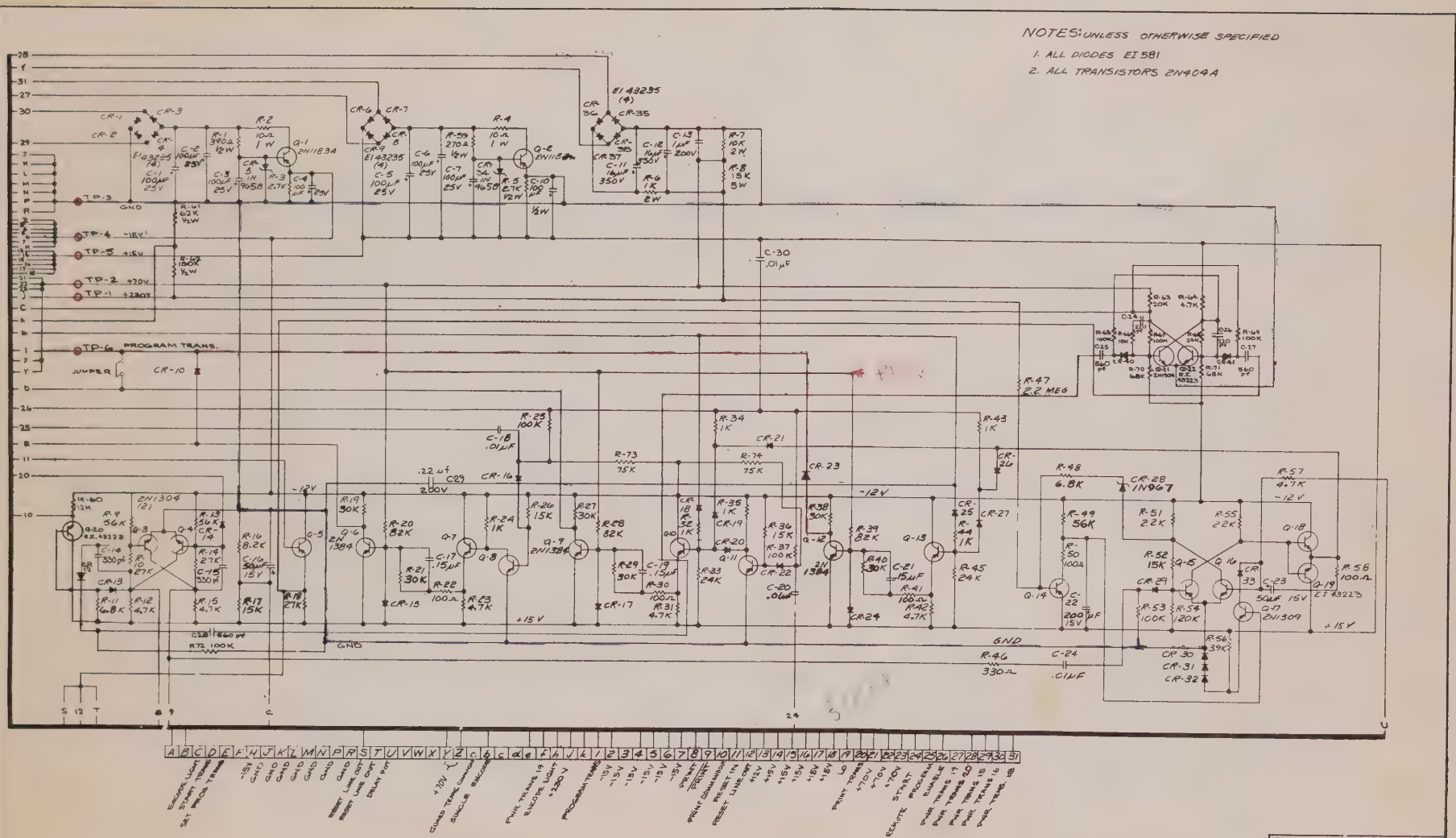


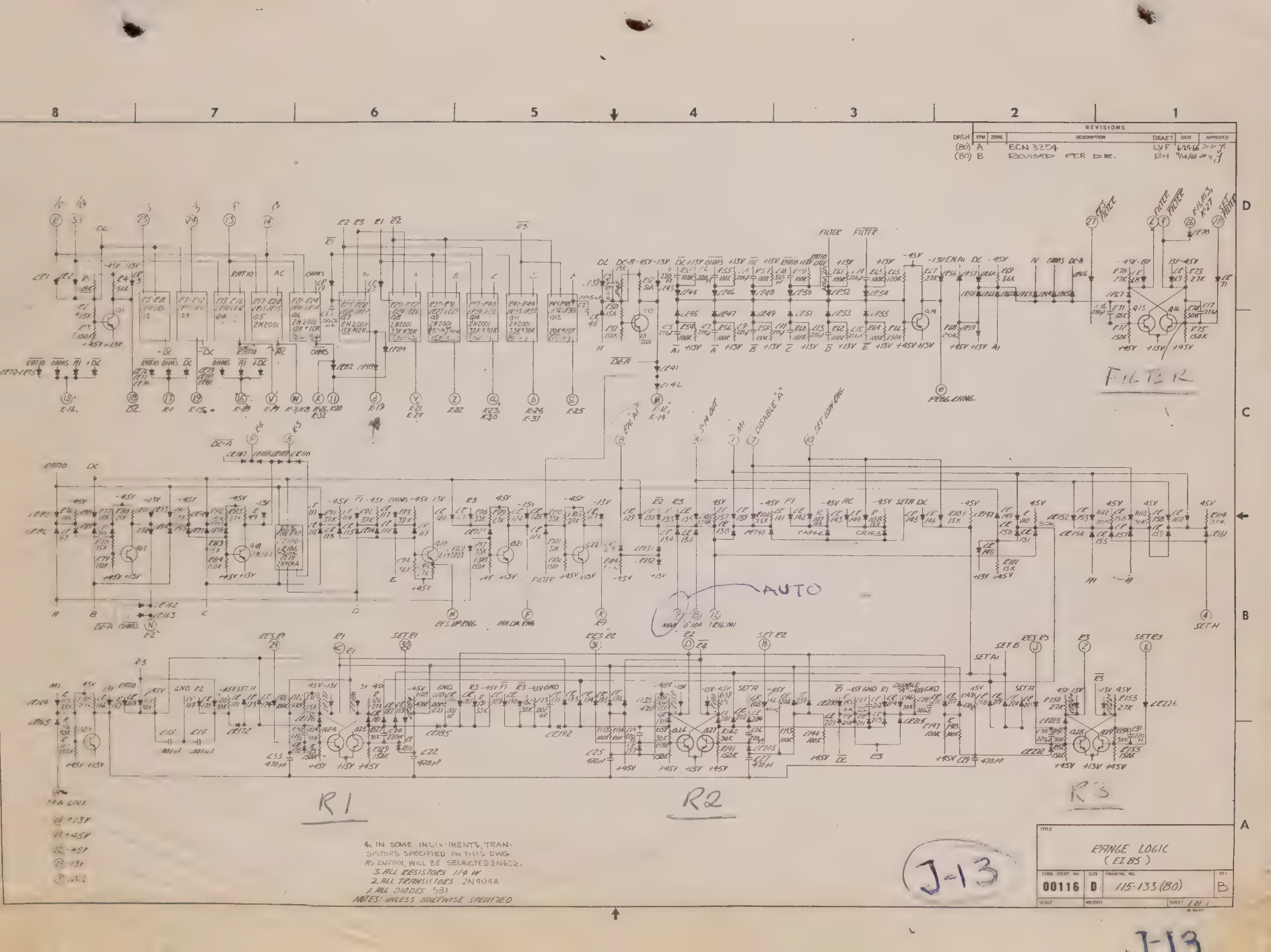
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS 1/4 W.
2. ALL LOGIC POS "TRUE" GND "FALSE".
3. ALL DIODES E.I. 561
4. Q-1 THRU Q-23 : E.I. 43223.

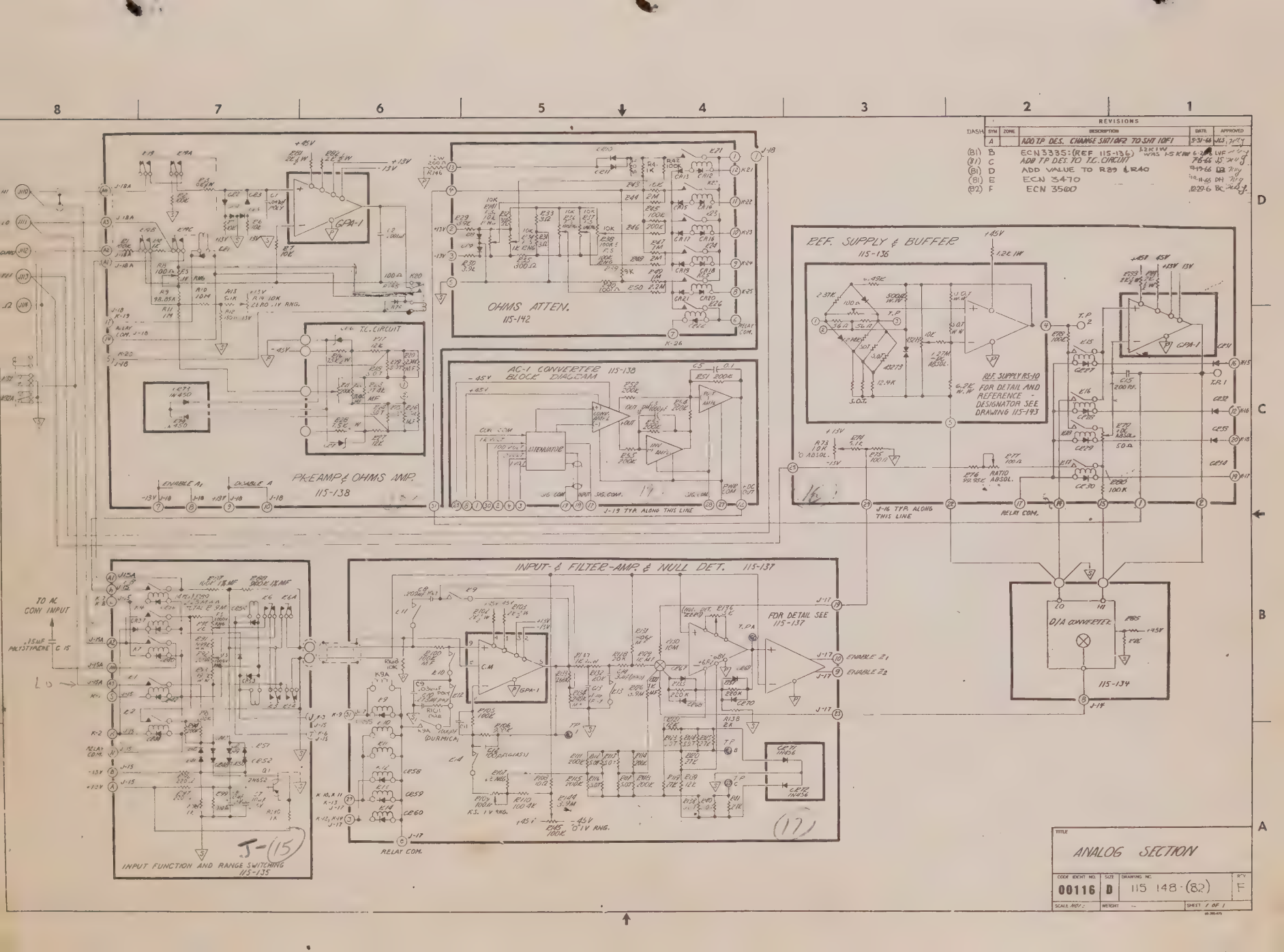
A' = .1v
A = 1v
B = 10v
C = 100v
D = 1000v

TITLE	DECADE & SYMBOL DRIVER EI-95
MATERIAL	J2
FINISH	
TOOL	SCALE NONE
NEXT ASSY.	TYPE SCHEMATIC
SHT. 1 OF 1	DWG. NO. 115-122 DASH (31)

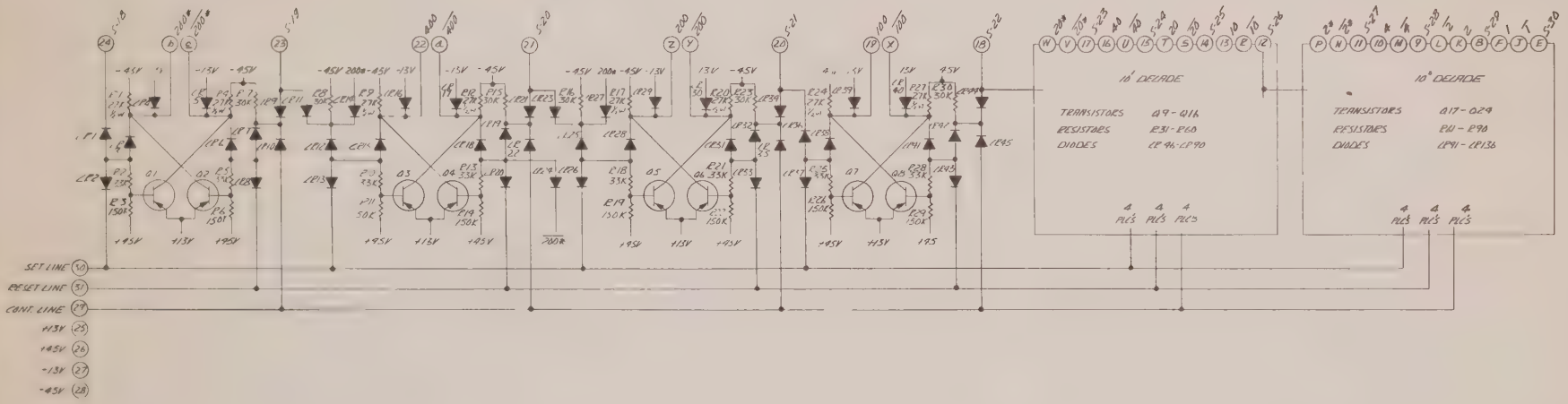
J2

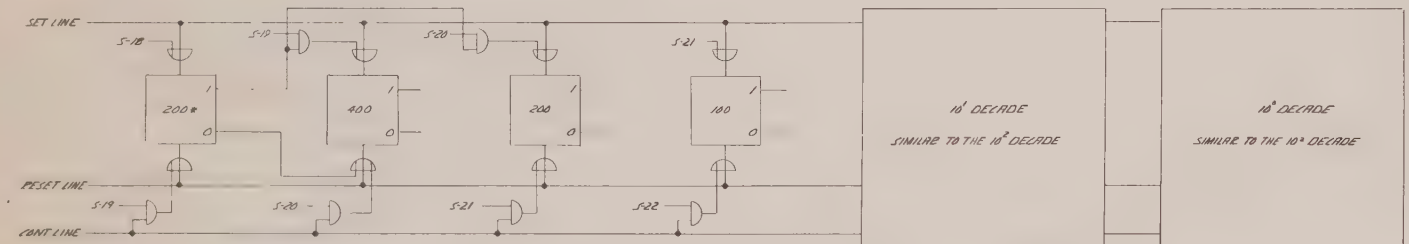

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL DIODES EI 581
2. ALL TRANSISTORS 2N404A
TP-3 GND
TP-4 -18V
TP-5 +15V
TP-2 +70V
TP-1 +230V
TP-6 PROGRAM TRANS.
JUMPER
CR-10
-12V
+15V
GND
OUTSIDE PWR. SUPPLY & CONTROL LOGIC - BOARD 1
EI 85
NONE
SCHEM.
115-121-80
SHT. 1 OF 1
115-121


8
7
6
5
4
3
2
1
REVISIONS
DASH | ZONE | DESCRIPTION | DRAFT | DATE | APPROVED
(80) A ECN 3254 LVF 6-24-66
(80) B REVISED PER DIE. DH 9/14/16
FILTER
FILTER
AUTO
R1
R2
R3
4. IN SOME INSTRUMENTS, TRANSISTORS SPECIFIED ON THIS DWG AS 2N2001, WILL BE SELECTED 2N682.
3. ALL RESISTORS 1/4 W
2. ALL TRANSISTORS 2N404A
1. ALL DIODES 581
NOTES: UNLESS OTHERWISE SPECIFIED
J-13
RANGE LOGIC
(E1.B5)
00116
D
115-133 (80)
B
J-13


REVISIONS
DASH | SYM | ZONE | DESCRIPTION | DATE | APPROVED
A | | | ADD TP DES. CHANGE SHT 1 OF 2 TO SHT 1 OF 1 | 5-31-66 | JLS
(B1) B | | | ECN 33351 (REF 115-136) WAS 1.5K 1W 2.2K 1W | 6-2-66 | JLS
(B1) C | | | ADD TP DES. TO I.C. CIRCUIT | 7-5-66 | JLS
(B1) D | | | ADD VALUE TO R39 & R40 | 9-17-66 | DH
(B1) E | | | ECN 3470 | 10-11-66 | DH
(B2) F | | | ECN 3500 | 10-29-68 | BC
PK-EAMP & OHMS AMP. 115-138
OHMS ATTEN. 115-142
AC-1 CONVERTER 115-138 BLOCK DIAGRAM
REF. SUPPLY & BUFFER 115-136
REF. SUPPLY RS-10 FOR DETAIL AND REFERENCE - DESIGNATOR SEE DRAWING 115-143
INPUT & FILTER-AMP. & NULL DET. 115-137
FOR DETAIL SEE 115-137
D/A CONVERTER
115-134
INPUT FUNCTION AND RANGE SWITCHING 115-135
J-15
TO AC CONV INPUT
RELAY COM.
J-19 TYP ALONG THIS LINE
J-16 TYP. ALONG THIS LINE
ENABLE A1
ENABLE A
DISABLE A
TITLE
ANALOG SECTION
CODE IDENT NO. 00116
SIZE D
DRAWING NO. 115 148-(82)
REV F
SCALE NONE
WEIGHT --
SHEET 1 OF 1

REVISIONS					
SYM	ZONE	DESCRIPTION	DATE	APPROVED	
130	A7	ELDORADO OLD DRAWING	7-73	CSB	



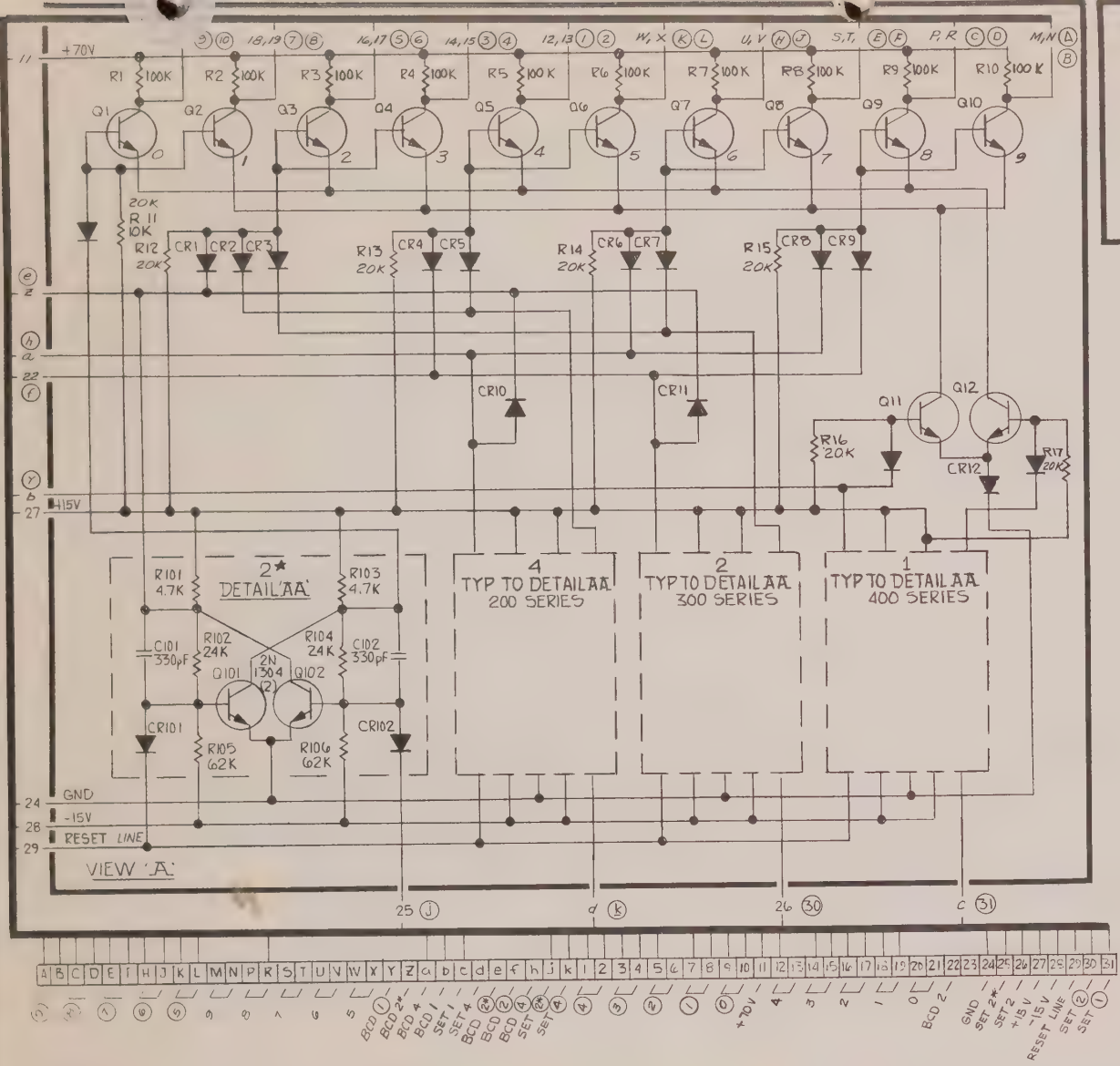


3 ALL RESISTORS 1/4W
2 ALL DIODES EE 5341
1 ALL TRANSISTORS 2N4041
NOTES: UNLESS OTHERWISE SPECIFIED

J10

TITLE				
10³ 10' 10° DECADE E.I. 85				
CODE IDENT NO	SIZE	DRAWING NO		REV
00116	D	115-130-(130)		A
SCALE ———	WEIGHT ———	SHEET 1 OF 1		

J10

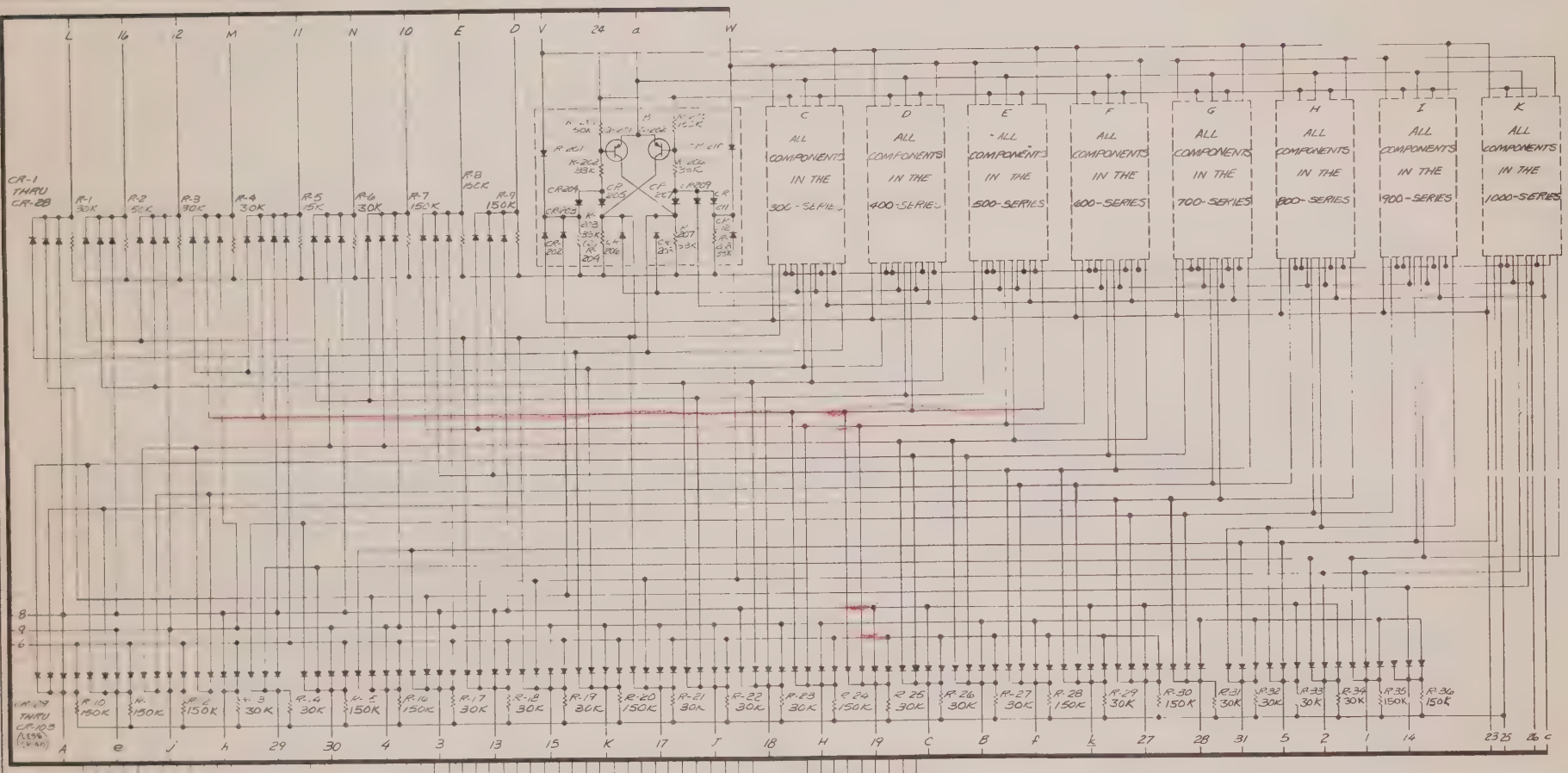


TYPICAL TO VIEW A

NOTE: NUMBERS IN ○ INDICATES PINS USED FOR THIS VIEW.

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL DIODES ARE EI 581
2. ALL RESISTORS AKE 1/4 WATT.
3. Q1 THRU Q12 IS EI 43223.

TITLE	DECADE & NIXIE DRIVER
MATERIAL	
FINISH	
TOOL	SCALE NONE
NEXT ASSY. 115-123-81	TYPE SCHEM.
SHT. 1 OF 1	DWG. NO. 115-123 DASH (80)

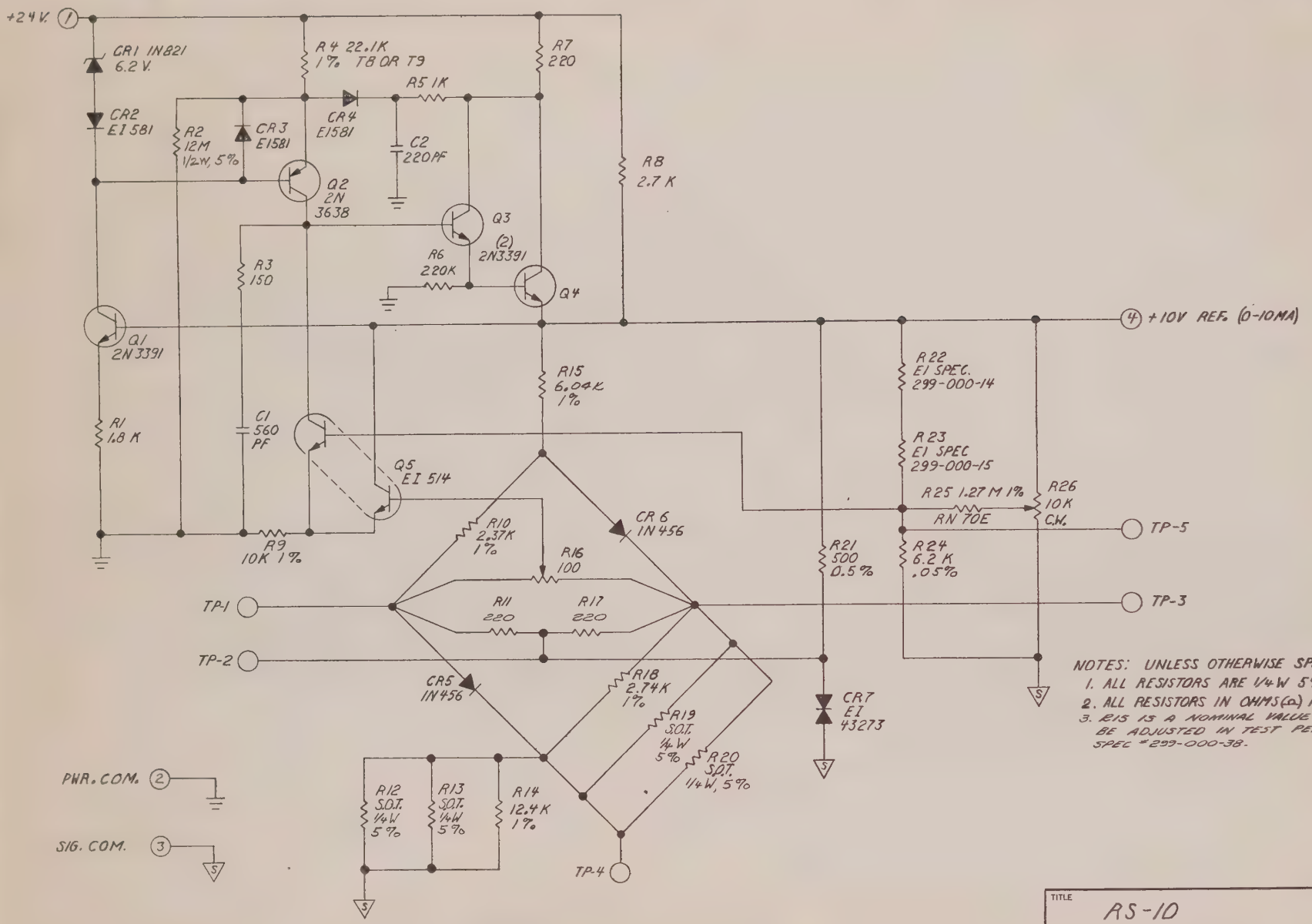


NOTES. UNLESS OTHERWISE SPECIFIED

1. ALL DIODES E1581
2. ALL TRANSISTORS 2N404A
3. ALL RESISTORS ¼ W

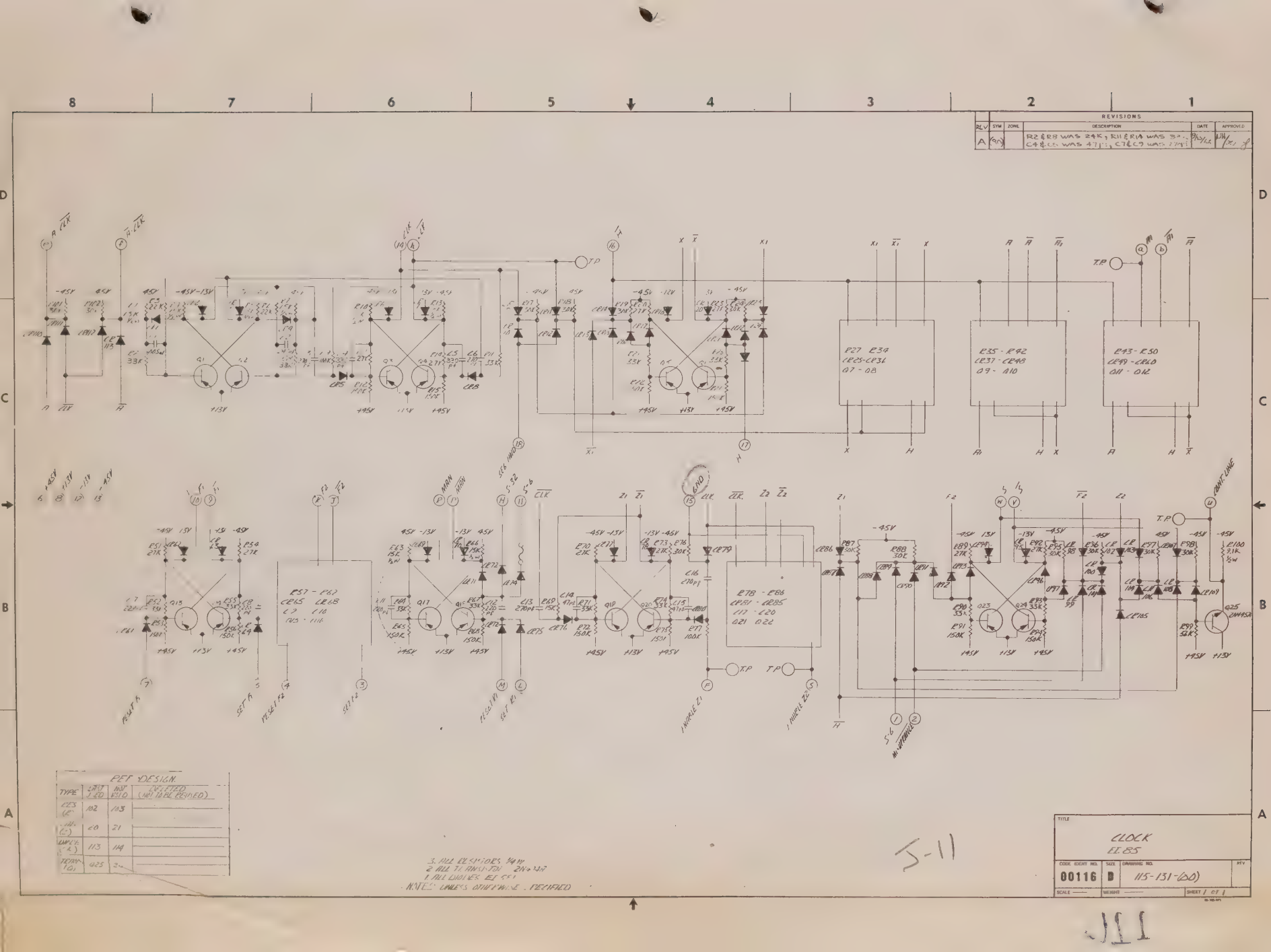
TITLE	SEQUENCER E.I.-85
MATERIAL	105-101-00
FINISH	
TOOL	SCALE NONE
NEXT ASSY	115-128-80
SHT. 1 OF 1	SIZE C
	DWG NO 115-128-(82)

SEQUENCER J-8



NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE 1/4 W 5% CARBON
2. ALL RESISTORS IN OHMS (Ω) K=1000 Ω
3. R15 IS A NOMINAL VALUE & MAY BE ADJUSTED IN TEST PER SOT SPEC #299-000-38.

TITLE: RS-10 REF. SUPPLY			
CODE IDENT NO. 00116	SIZE C	DRAWING NO. 115-143-(81)	REV H
SCALE NONE	WEIGHT	SHEET 1 OF 1	


REVISIONS
REV SYM ZONE DESCRIPTION DATE APPROVED
A R2 & R8 WAS 24K; R11 & R14 WAS 3.3K; C4 & C10 WAS 47pf; C7 & C9 WAS 27pf
P27 E34 LE25-LE31 Q7 - Q8
E35 - E92 LE37 - LE43 Q9 - A10
E93 - E50 LE49 - LE55 Q11 - Q12
E57 - E62 LE45 LE48 C2 C10 Q5 - Q6
E78 - E86 LE51 - LE85 C17 - C20 Q21 Q22
PET DESIGN
TYPE | SAY 1 LED | NOT USED | INSERTED (NO) TO BE REMOVED
LE25 (C) | 102 | 103
LE45 (C) | 20 | 21
LE46 (C) | 113 | 114
TEXAS T01 | 425 | 3-11
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS 1/4 W
2. ALL TRANSISTORS 2N4037
3. ALL DIODES IN4148
TITLE
CLOCK LE85
CODE IDENT NO. 00116
SIZE B
DRAWING NO. 115-131-(50)
REV
SCALE
WEIGHT
SHEET 1 OF 1
5-11

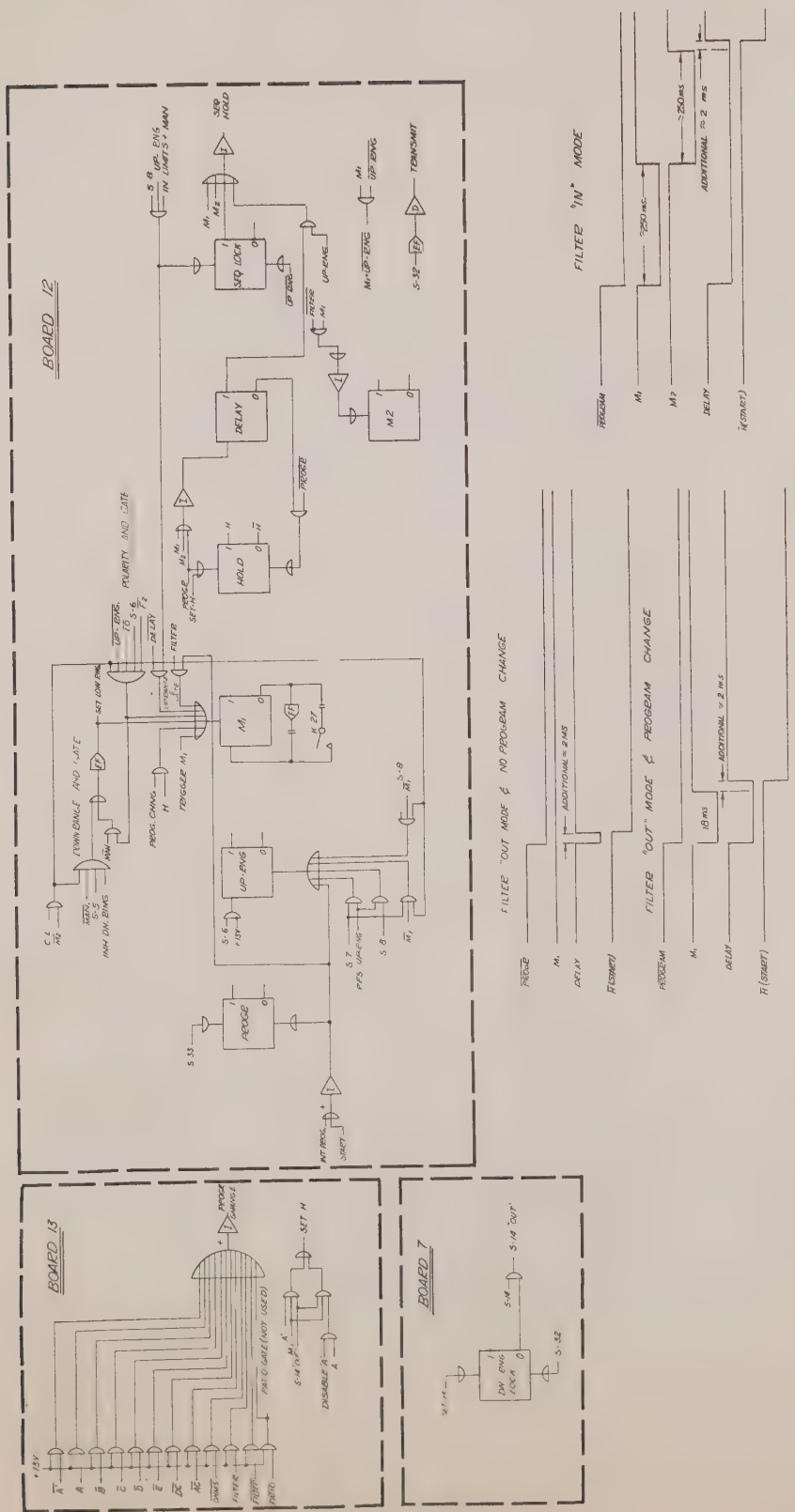


Figure 3.12. Guarded Program and Control Logic and Sequence Delay Waveforms

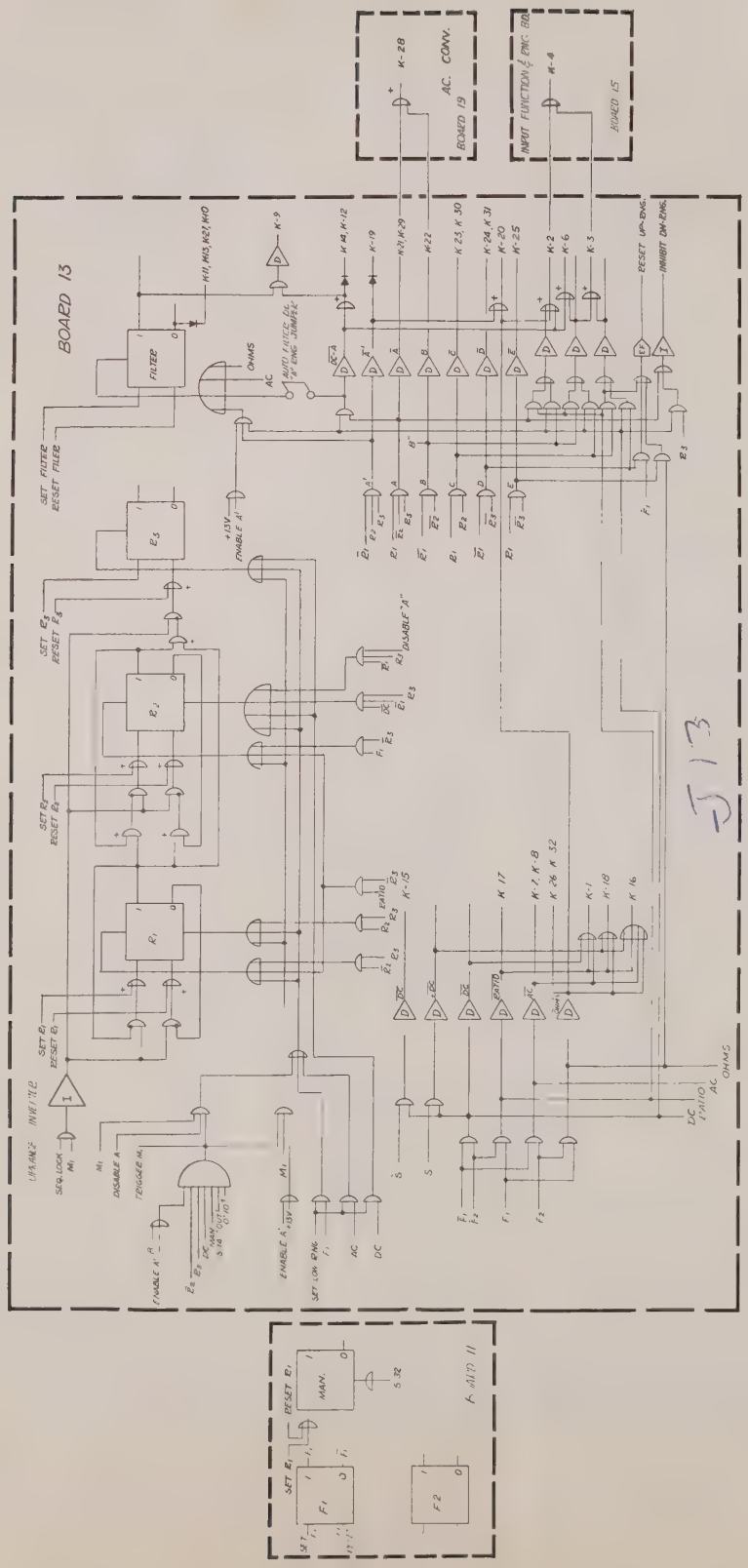
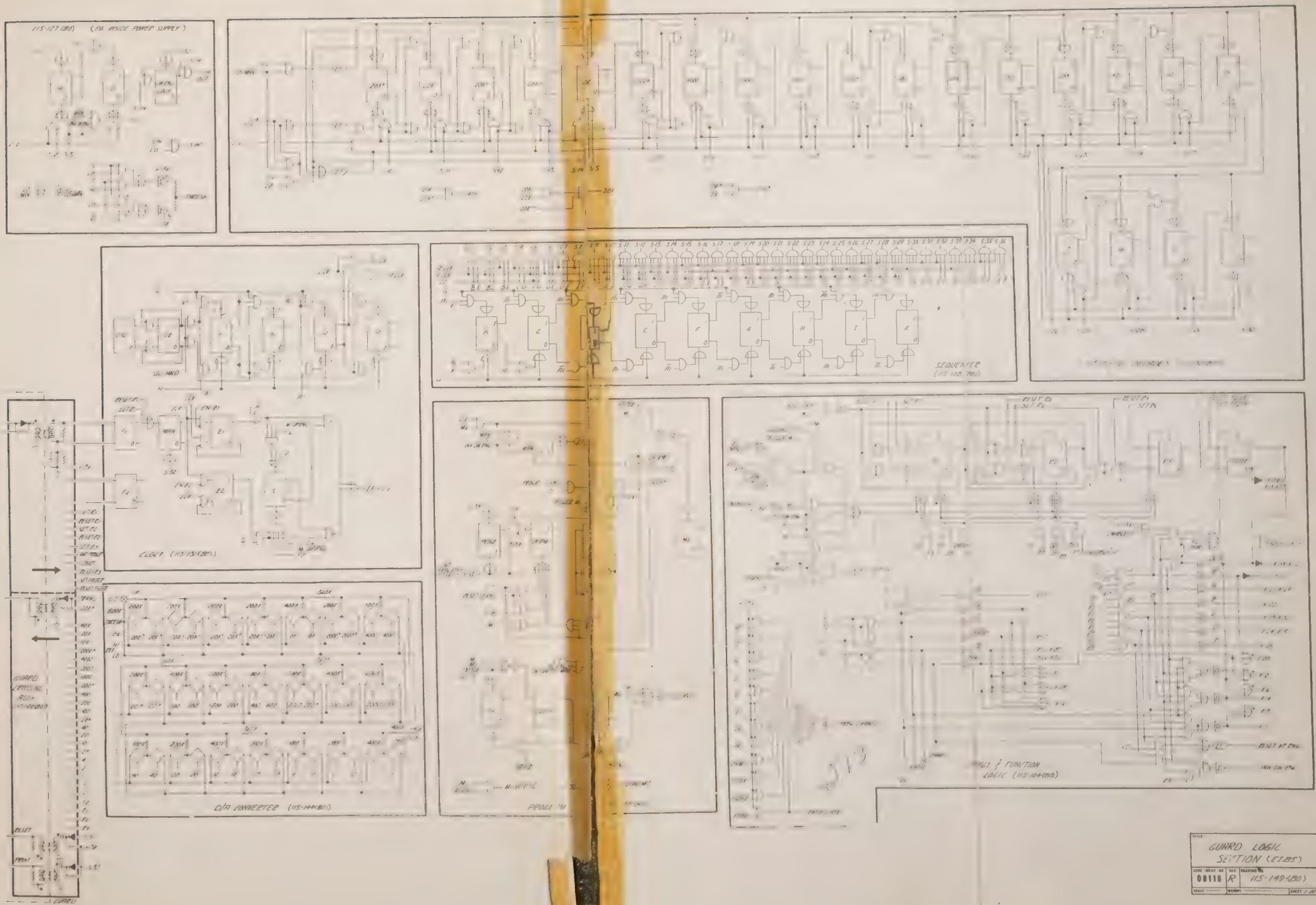
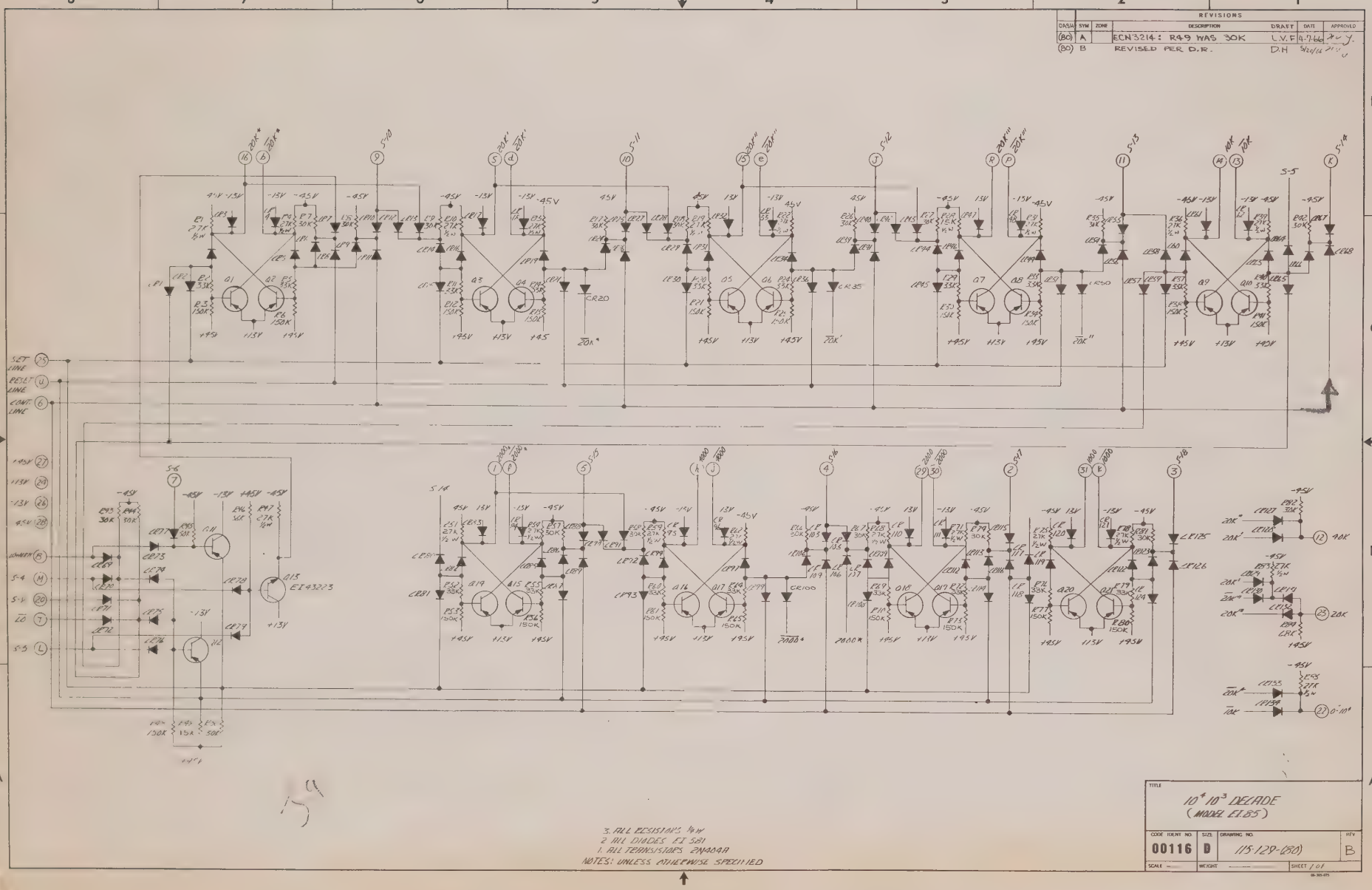
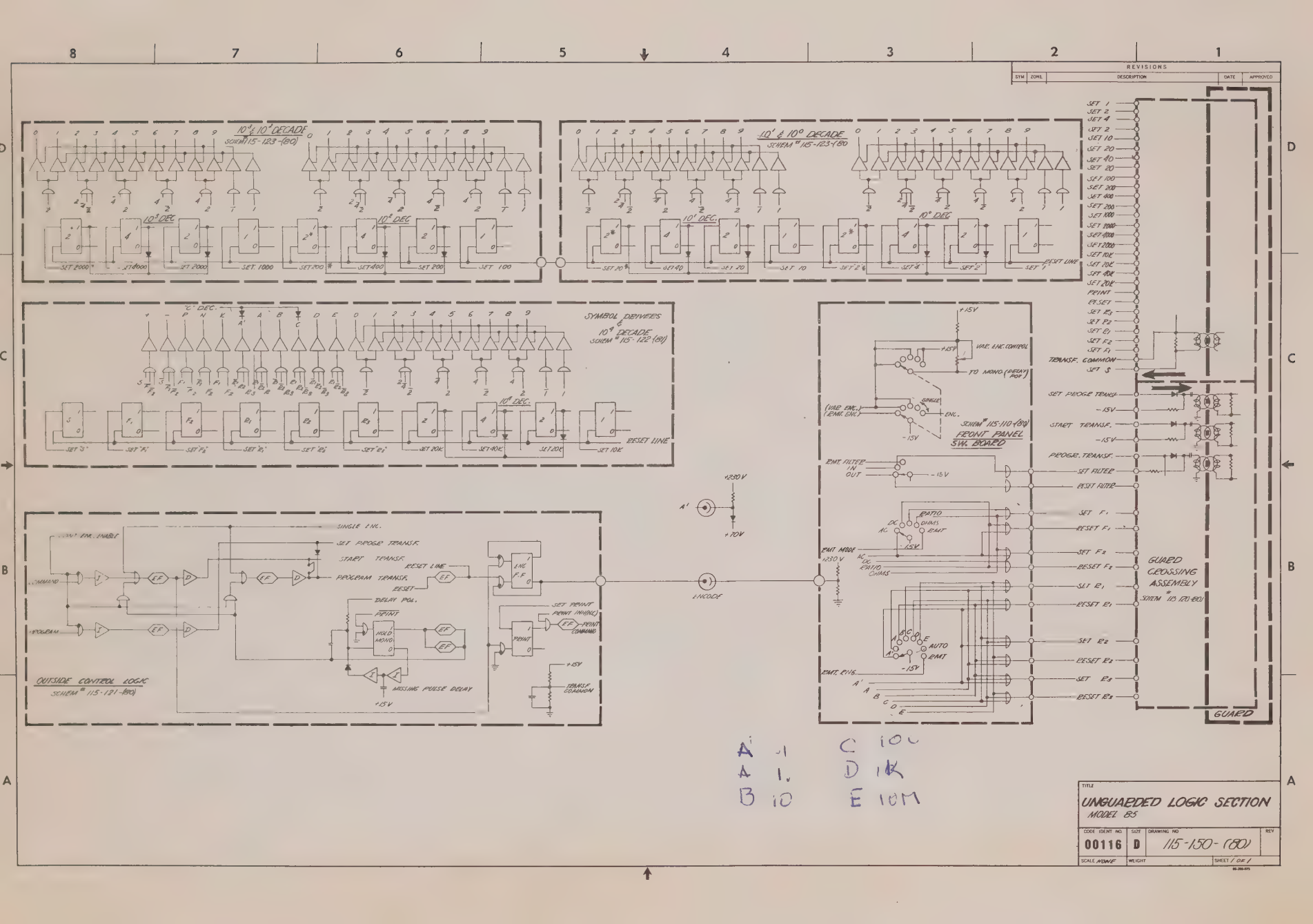
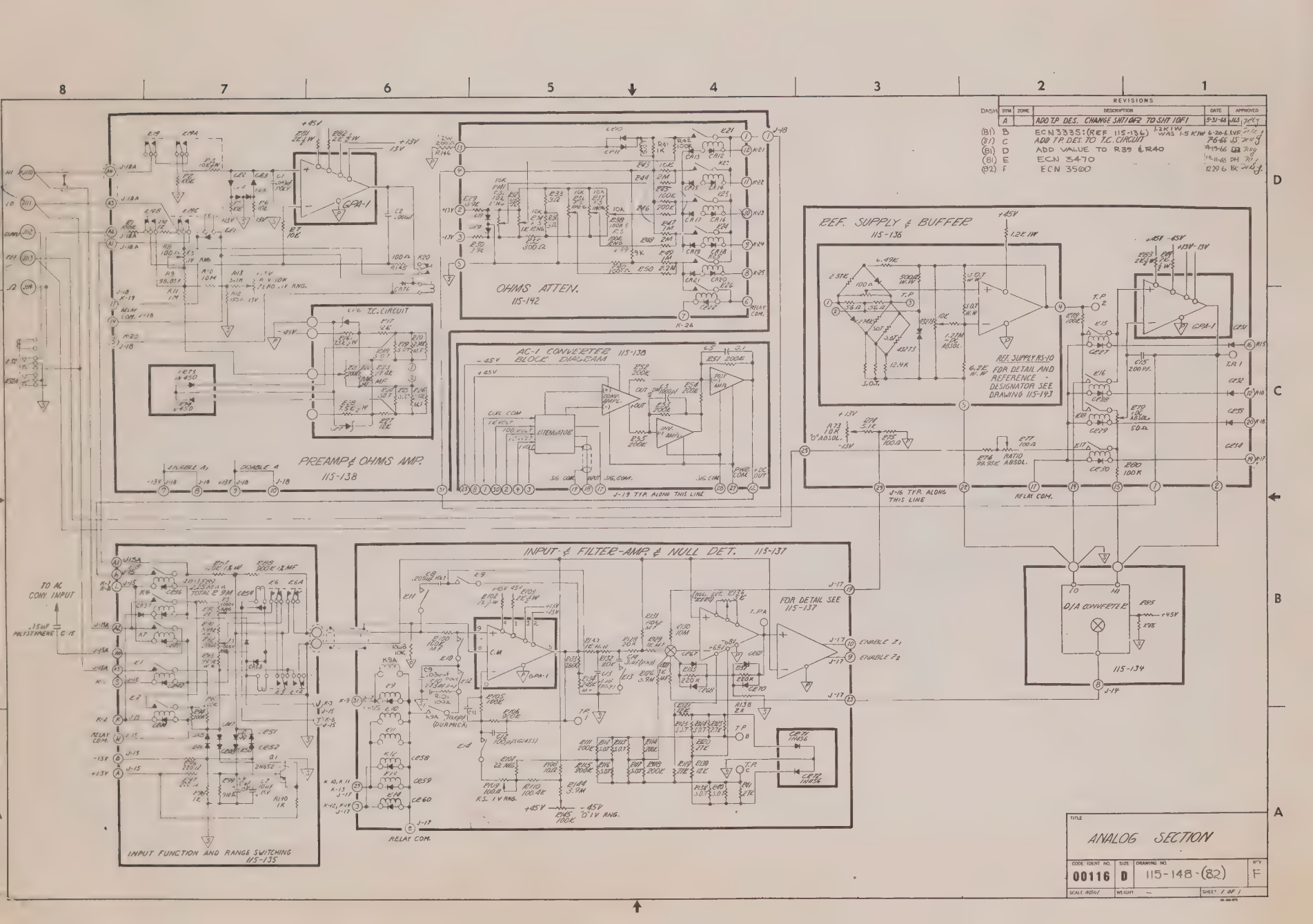


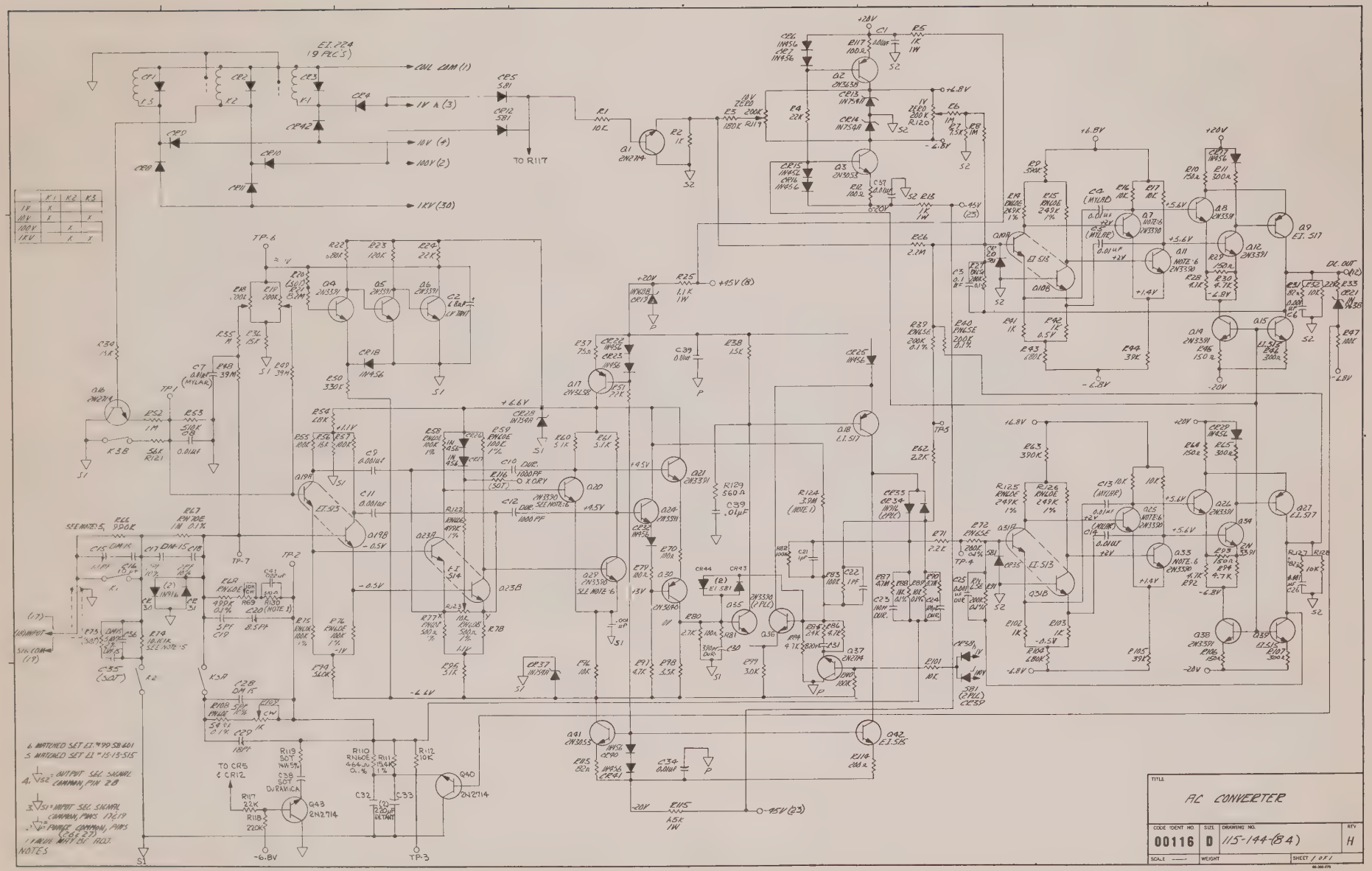
Figure 3.13. Relay Drivers, Range and Function Logic


115-127 (B0) (PA INSIDE POWER SUPPLY)
SEQUENCER (115-128 (B0))
CLOCK (115-154 (B0))
D/A CONVERTER (115-149 (B0))
PROGRAM
GUARD LOGIC & FUNCTION LOGIC (115-104 (B0))
GUARD (PROGRAM) (115-148 (B0))
GUARD
RESET
PROGRAM
GUARD LOGIC SECTION (EXT. BUS)
00116
115-149 (B0)


REVISIONS
DASH | SYM | ZONE | DESCRIPTION | DRAFT | DATE | APPROVED
(80) A ECN3214: R49 WAS 30K L.V.F 4-7-66
(80) B REVISED PER D.R. D.H 5/26/66
SET LINE
RESET LINE
CONT. LINE
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10
Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20
Q21 Q22
EI 43223
CR20
CR35
CR100
CR125
CR126
3. ALL RESISTORS ½W
2. ALL DIODES EI 581
1. ALL TRANSISTORS 2N404A
NOTES: UNLESS OTHERWISE SPECIFIED
TITLE
10⁴ 10³ DECADE
(MODEL EI 85)
CODE IDENT NO. 00116
SIZE D
DRAWING NO. 115-129-(80)
REV B
SCALE
WEIGHT
SHEET 1 OF 1


REVISIONS
SYM | ZONE | DESCRIPTION | DATE | APPROVED
10⁴ & 10³ DECADE
SCHEM # 115-123-(80)
10² DEC.
10¹ DEC.
10⁰ DECADE
SCHEM # 115-123-(80)
SET 2000
SET 1000
SET 200
SET 400
SET 100
SET 40
SET 20
SET 10
SET 4
SET 2
SET 1
RESET LINE
SYMBOL DRIVERS &
10⁴ DECADE
SCHEM # 115-122-(81)
SET 20K
SET 40K
SET 10K
SET 'S'
SET 'A'
SET 'B'
SET 'C'
SET 'D'
SET 'E'
+15V
VAR. FNC. CONTROL
TO MONO (DELAY) PCT
SINGLE
ENC.
-15V
SCHEM # 115-110-(80)
FRONT PANEL
SW. BOARD
EMIT FILTER
IN
OUT
RATIO
DC
AC
OHMS
EMIT
EMIT MODE
230 V
EMIT RNG.
AUTO
SET FILTER
RESET FILTER
SET F1
RESET F1
SET F2
RESET F2
SET E1
RESET E1
SET E2
RESET E2
SET E4
RESET E4
TRANSF. COMMON
SET S
SET PROGR. TRANSF.
START TRANSF.
PROGR. TRANSF.
GUARD CROSSING ASSEMBLY
SCHEM # 115-121-(80)
GUARD
SINGLE ENC.
SET PROGR. TRANSF.
START TRANSF.
RESET LINE
PROGRAM TRANSF.
RESET
DELAY POT.
PRINT
HOLD MONO
SET POINT
PRINT INHIBIT
PRINT COMMAND
TRANSF. COMMON
MISSING PULSE DELAY
ENC. F.F.
OUTSIDE CONTROL LOGIC
SCHEM # 115-121-(80)
ENCODE
230V
10V
A' .1
A 1.
B 10
C 100
D 1K
E 10K
TITLE
UNGUARDED LOGIC SECTION
MODEL 85
CODE IDENT NO. 00116
SIZE D
DRAWING NO. 115-150-(80)
REV
SCALE NONE
WEIGHT
SHEET 1 OF 1


REVISIONS
DASH | SYM | ZONE | DESCRIPTION | DATE | APPROVED
A | | ADD TP DES. CHANGE SHT 1 OF 2 TO SHT 1 OF 1 | 5-31-66 | WLS
(B1) B | | ECN 3335: (REF 115-136) 1.2K 1W WAS 1.5 K1W | 6-20-66 | LVF
(B1) C | | ADD TP DES. TO T.C. CIRCUIT | 7-6-66 | WLS
(B1) D | | ADD VALUE TO R39 & R40 | 9-19-66 | WLS
(B1) E | | ECN 3470 | 10-11-66 | DH
(B2) F | | ECN 3500 | 12-29-6 | BC
PREAMP & OHMS AMP. 115-138
OHMS ATTEN. 115-142
AC-1 CONVERTER 115-138 BLOCK DIAGRAM
REF. SUPPLY & BUFFER 115-136
REF. SUPPLY RS-10 FOR DETAIL AND REFERENCE DESIGNATOR SEE DRAWING 115-143
INPUT & FILTER-AMP. & NULL DET. 115-137
FOR DETAIL SEE 115-137
INPUT FUNCTION AND RANGE SWITCHING 115-135
D/A CONVERTER 115-134
TO AC CONV. INPUT
RELAY COM.
ANALOG SECTION
00116
115-148-(82)
F


AC CONVERTER
00116
D
115-144-(84)
H
SCALE
WEIGHT
SHEET 1 OF 1
+28V
+6.8V
+20V
-6.8V
-20V
-45V (23)
+45V (8)
-6.8V
-6.8V
-20V
-6.8V
-6.8V
-6.8

MODEL GPA-1
GENERAL PURPOSE AMPLIFIER
APPENDIX NO. 1

The material contained in this document may not be reproduced in any form without written permission from Electro Instruments, Inc.

TABLE OF CONTENTS

Paragraph No.		Page
	SECTION I - DESCRIPTION	
A1.1	Introduction	A1.1
A1.2	Function	A1.1
	SECTION II - OPERATION	
A2.1	Preliminary Checks	A2.1
A2.2	Circuit Configurations and Options	A2.1
A2.2.1	Voltage Supply Requirements	A2.1
A2.2.2	Feedback Circuits	A2.7
A2.2.3	Remote Sensing	A2.7
A2.2.4	Common Mode Guard	A2.7
A2.3	Installation	A2.7
	SECTION III - THEORY OF OPERATION	
A3.1	Principle of Operation - General	A3.1
A3.1.1	Operational Mode, Figure A3.1(a)	A3.2
A3.1.2	Potentiometric Mode, Figure A3.1(b)	A3.2
A3.2	Input/Output Considerations	A3.2
A3.2.1	Single-Ended/Differential Inputs	A3.2
A3.2.2	Common Mode/Normal Mode	A3.3
A3.2.3	Input Bootstrapping	A3.4
A3.2.4	Four-Wire Output	A3.5
A3.2.5	Integration	A3.6
A3.3	Circuit Description	A3.6
A3.3.1	General	A3.7
A3.3.2	Amplifier K1	A3.7
A3.3.3	Amplifier K2	A3.7
A3.3.4	Amplifier K3	A3.8
A3.3.5	Amplifier K4	A3.8
A3.3.6	Constant Current Supplies	A3.8
	SECTION IV - CALIBRATION	
A4.1	General	A4.1
A4.2	Construction of Test Fixture	A4.1
A4.3	Calibration of Test Fixture	A4.3
A4.4	Offset Adjustments	A4.5

TABLE OF CONTENTS (Continued)

Paragraph No.		Page
	SECTION V - MAINTENANCE	
A5. 1	General	A5. 1
A5. 2	Test Equipment Required	A5. 1
A5. 3	Test Procedure	A5. 1
A5. 4	Corrective Maintenance	A5. 2
A5. 5	Replacement of Trim Resistors	A5. 3
A5. 5. 1	Current Offset Trim Resistor R3'	A5. 3
A5. 5. 2	Voltage Offset Trim Resistor R26	A5. 5

LIST OF ILLUSTRATIONS

Figure Number	Title	Page
A2.1	Block Diagram, GPA-1	A2.2
A2.2	Inverting Amplifier, GPA-1 (Using Gain Determining Impedances on Board)	A2.3
A2.3	Non-Inverting Amplifier, GPA-1 (Using Gain Determining Impedances on Card)	A2.4
A2.4	Inverting Amplifier, GPA-1 (Using External Gain Impedances)	A2.5
A2.5	Inverting Amplifier, GPA-1 Remote Sensing (Using Gain Determining Impedances on Card)	A2.6
A3.1	Basic Amplifier Configurations	A3.1
A3.2	Subtractor (Modified Operational Amplifier)	A3.3
A3.3	Voltage Follower (Modified Potentiometric Amplifier)	A3.4
A3.4	Input Bootstrapping	A3.4
A3.5	Operational Amplifier (Showing Line Resistances)	A3.5
A3.6	Operational Amplifier (With Four-Wire Output)	A3.5
A3.7	Integrator	A3.6
A3.8	Simplified Diagram - Model GPA-1 General Purpose Amplifier	A3.7
A4.1	Improvised GPA-1 Test Fixture	A4.2
A4.2	GPA-1 Printed Circuit Board	A4.4
A5.1	Location of Trim Resistor R26	A5.6

LIST OF TABLES

Table Number	Title	Page
A5.1	Selection of R3' (R3 = 10 megohm)	A5.5
A5.2	Selection of R26	A5.6

SECTION I

DESCRIPTION

A1.1 INTRODUCTION

The Model GPA-1 General Purpose Amplifier is a direct-coupled plug-in amplifier than can be used with external (or internal) add-on impedances as an integral part of a larger analog circuit. The impedance configuration determines the gain and function of the integrated circuit. The amplifier input is differential with high common mode input impedance, providing good operation and low current uncertainties from high resistance sources. DC drift with temperature is minimized within the amplifier; however provision is made for installing temperature compensating diodes on the input pair transistor heat sink as part of an external temperature compensation bridge. If the temperature compensation circuit is not used, the amplifier plug-in boards can be exchanged without re-calibration. If the temperature compensation circuit is used, it should be readjusted. The amplifier is normally used without chopper stabilization. (There is a patent pending on circuits used in the amplifier.)

A1.2 FUNCTION

The amplifier can operate in an inverting or non-inverting mode, i. e. operational or potentiometric, depending on the signal and feedback connections. Other amplifier configurations for specific applications can be obtained by the addition of various circuit components.

The closed loop gain of the amplifier is determined by the value of the feedback impedance and the input impedance. Space is provided on the board for these two gain determining impedances, however, they are often mounted external to the amplifier. Gain switching can be accomplished by external circuits.

SECTION II

OPERATION

A2.1 PRELIMINARY CHECKS

As an integral part of an E. I. instrument, the GPA-1 amplifier is prepared with jumpers and/or feedback impedances previous to installation at the factory. When a replacement amplifier is ordered from the factory with reference to a specific instrument and circuit by instrument model and serial numbers and the circuit name, the amplifier can be installed in the instrument for immediate use. However, when a raw amplifier board is obtained from stock, or a board from another instrument is used (where the external-internal circuit wiring may be different), the board must be modified before use. Often, identical circuit configurations are used within an instrument and boards can be readily exchanged.

NOTE

When applicable, a readjustment of the external temperature compensation circuit becomes necessary after changing an amplifier board.

A2.2 CIRCUIT CONFIGURATIONS AND OPTIONS

A simplified block diagram of the basic amplifier board, with input/output terminal connections is shown in figure A2.1. The logic diagram of the instrument in which a particular amplifier is used will show which pins (or functions) are used and in what manner they are connected. Note that various options are provided which may or may not be incorporated in a particular instrument. The instrument logic diagram should be compared with the simplified diagrams showing examples of the various wiring configurations, figures A2.2 through A2.5, to determine which options are used in the instrument. Options are discussed below:

A2.2.1 Voltage Supply Requirements

The amplifier has a basic voltage supply requirement of + and - 24 volts. This can be used to operate the entire amplifier, or as an optional feature, the output stage power can be supplied from another voltage source to take some of the load from the main supply. The output current can be supplied by a lower voltage reducing the dissipation in the output transistors. When a separate supply is used for the output stage, jumpers 2 and 3 are removed, and the voltage is applied to pin 10 (Ext. +) and pin 11 (Ext. -). The external voltage should be

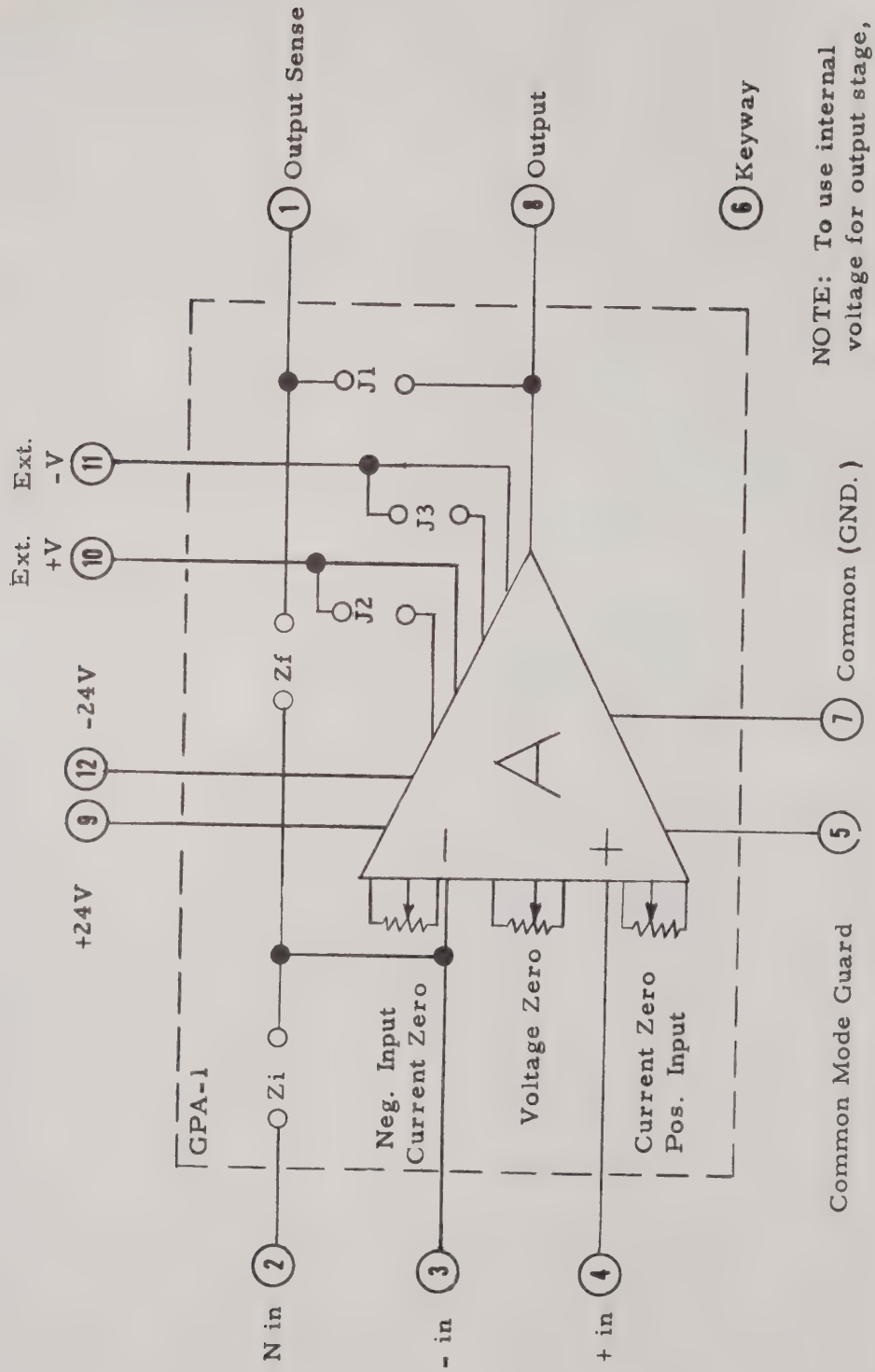


Figure A2.1 - Block Diagram, GPA-1

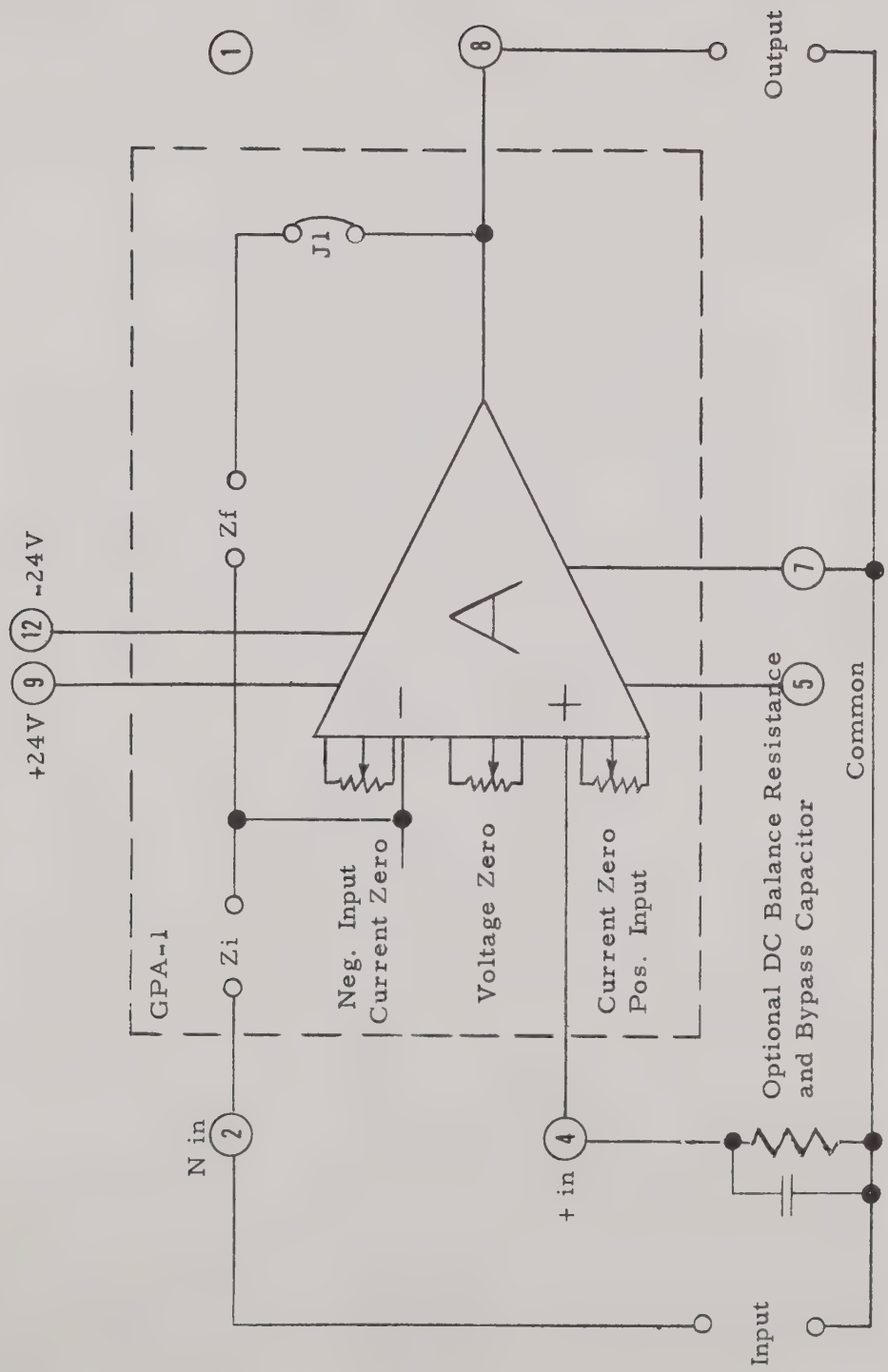


Figure A2.2 - Inverting Amplifier, GPA-1 (Using Gain Determining Impedances on Board)

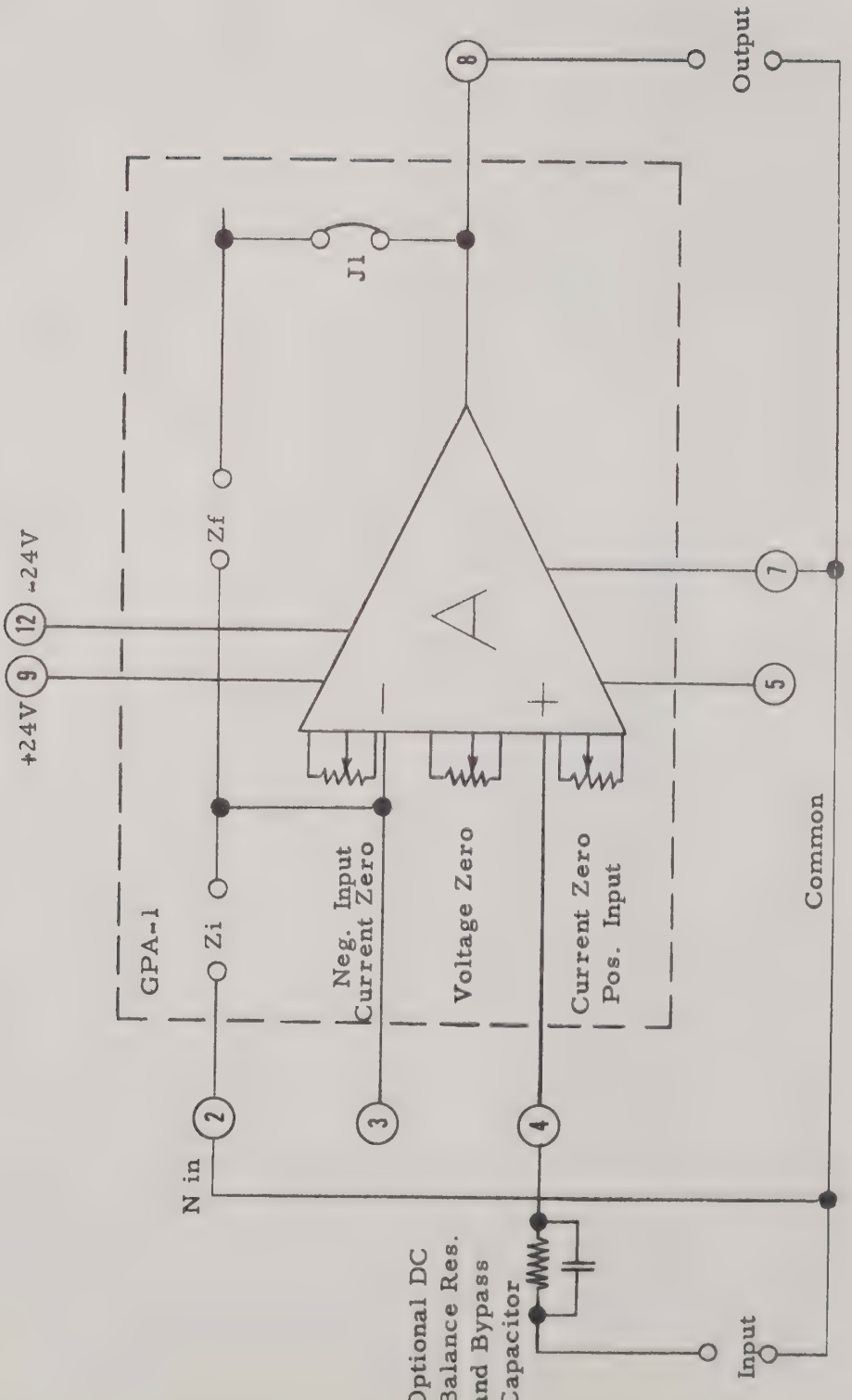


Figure A2. 3 - Non-Inverting Amplifier, GPA-1 (Using Gain Determining Impedances on Card)

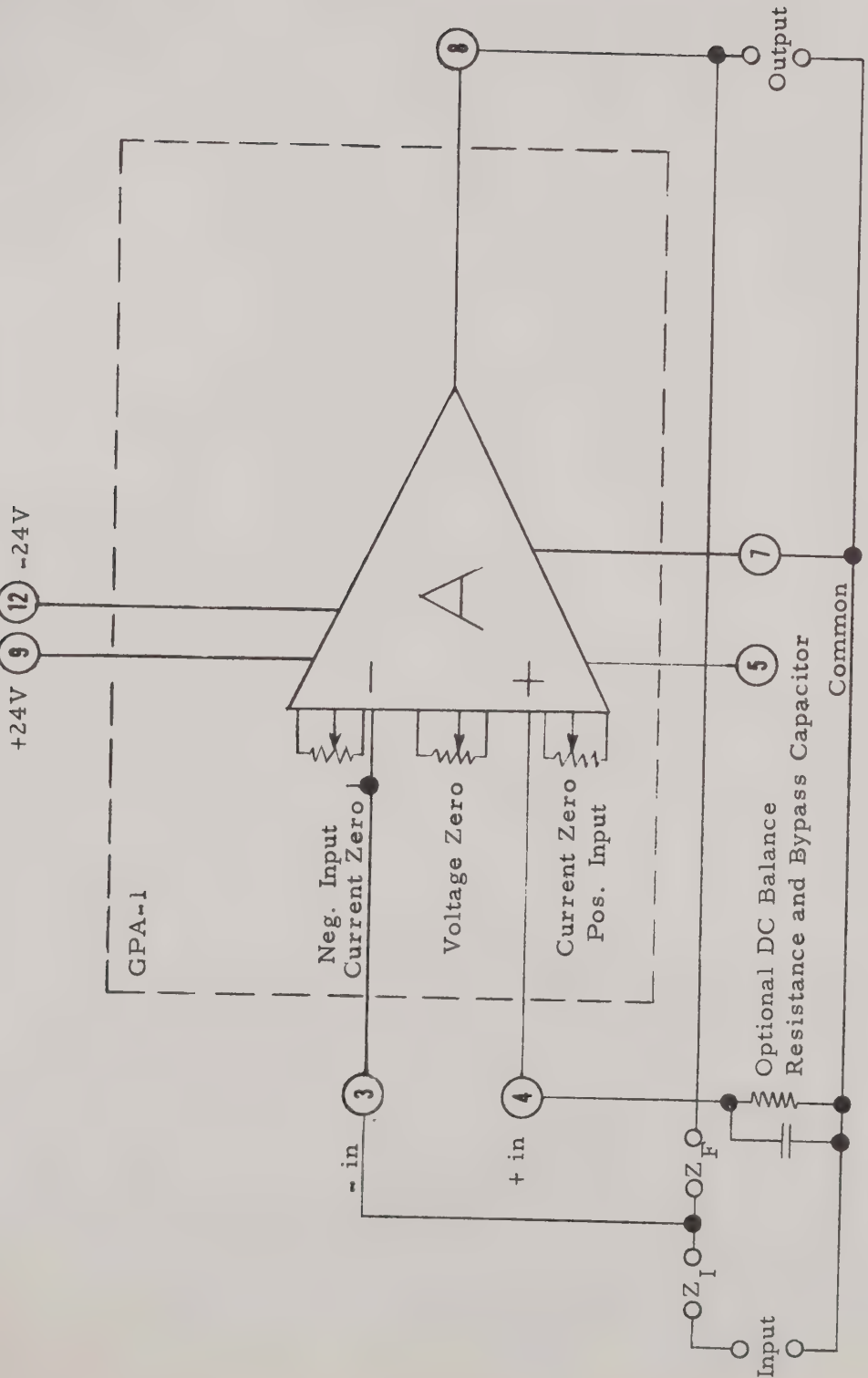


Figure A2.4 - Inverting Amplifier, GPA-1 (Using External Gain Impedances)

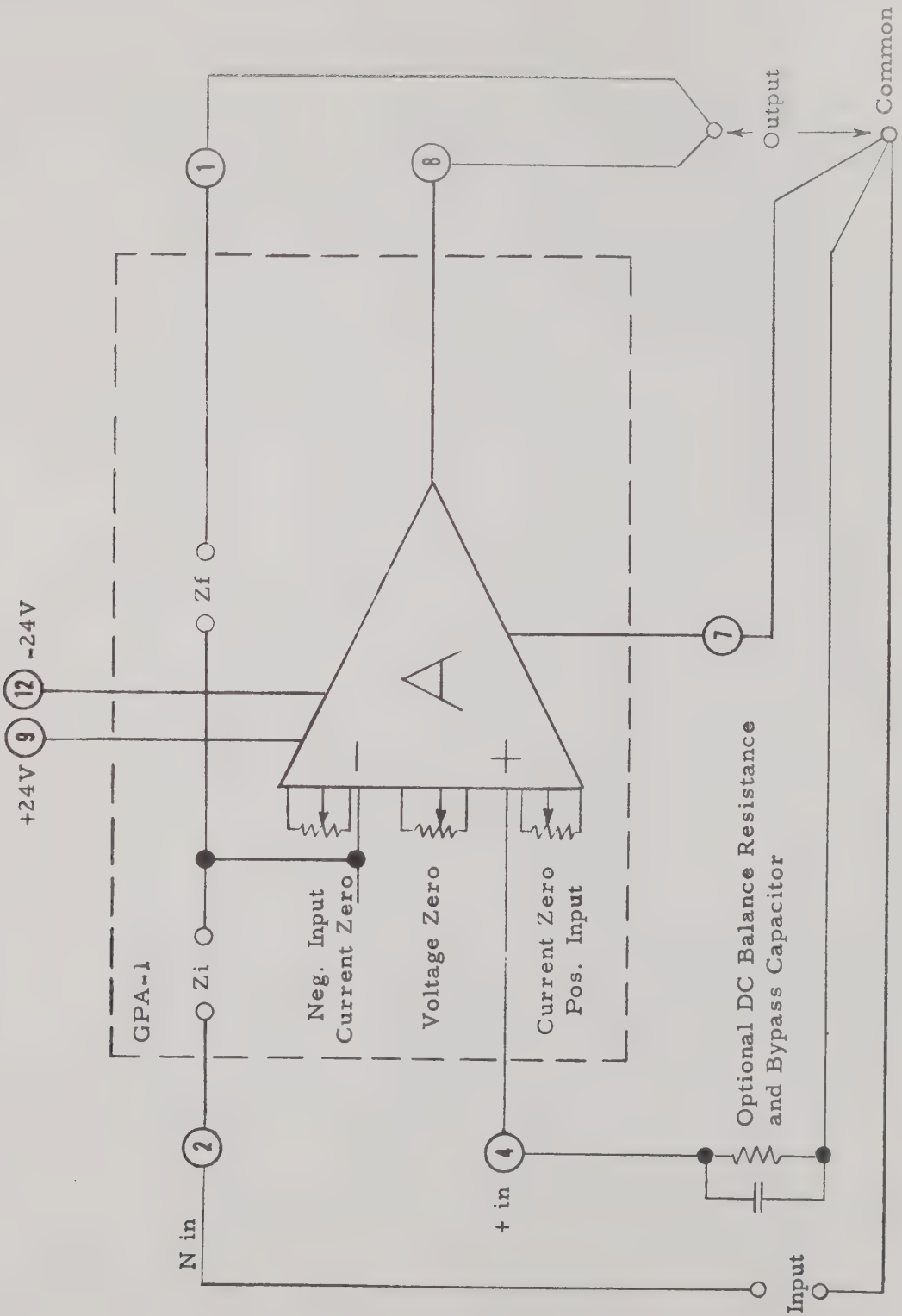


Figure A2.5 - Inverting Amplifier, GPA-1 Remote Sensing (Using Gain Determining Impedances on Card)

±2 volts greater than the maximum amplifier output (not to exceed ±12V). When the amplifier is operated entirely from the + and - 24 volt supplies, the jumpers are installed.

NOTE

Since the supply voltages are not always shown on logic diagrams, it may be necessary to refer to the instrument schematic to determine whether this option is used.

A2.2.2 Feedback Circuits

The feedback circuit can be installed on the board (in spaces provided), or external to the amplifier. The configuration of the feedback circuit determines the amplifier mode (inverting or non-inverting) and the value of the impedances determines the closed loop gain. In the operational mode the gain is approximately $-Z_f/Z_i$; in the potentiometric mode the gain is approximately $1 + Z_f/Z_i$. When the feedback circuit (gain determining impedances) is installed on the board, terminal 2 (N in) is used as the high or low side of the signal input depending on the amplifier mode.

A2.2.3 Remote Sensing

The amplifier output can be wired as a four-wire system by connecting the output sense point, terminal 1, to the high side of the output load and the low side of the input signal to the low side of the output load (common). When this option is used, jumper 1 should be removed. For two-wire output configurations, jumper 1 should be installed. (Refer to paragraph A3.2.4.)

A2.2.4 Common Mode Guard

A common mode guard terminal is provided. This terminal is driven by the amplifier at the common mode voltage and can be connected to an input shield, thus reducing the effects of common signal impedances to ground (refer to paragraph A3.2.3).

A2.3 INSTALLATION

After the appropriate modifications have been performed (if required), the amplifier can be plugged into the circuit. When a temperature compensation circuit is used, ensure that a good thermal bond is maintained between the diode assembly and the input pair transistor heat sink by means of the screws and mounting plate (do not use silicone grease). Readjust the temperature compensation bridge as outlined in Section IV of the instruction manual for the instrument (in which the circuit is used).

SECTION III

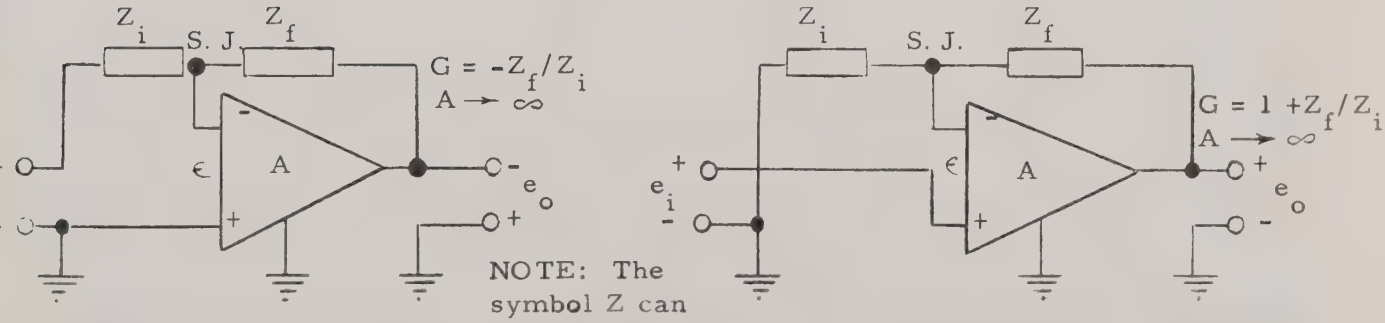
THEORY OF OPERATION

A3.1 PRINCIPLE OF OPERATION - GENERAL

The high open loop gain of the Model GPA-1 General Purpose Amplifier makes it ideally suited for feedback amplifier applications. The two basic feedback amplifiers, inverting (operational) and non-inverting (potentiometric) are illustrated in simplified form in figure A3.1. Each amplifier configuration performs two functions: it determines the polarity of the output signal, and the magnitude with respect to the input (gain). The polarity of the output depends on whether the signal high or signal low side is connected to the + (non-inverting) input of the amplifier. In figure (a), operational configuration, the signal low is connected to the non-inverting input and the signal is inverted. In figure (b), potentiometric configuration, the signal high is connected to the non-inverting input and the signal is not inverted. The closed loop gain of each amplifier is computed using the ratio of the impedances in the feedback loop, as given by the formulas in the illustrations. Derivations of these formulas are given in the following two paragraphs.

NOTE

The value of A is a complex quantity. Also, Z_i and Z_f can be complex, so that G would be complex, However, for purposes of explanation, all symbols are assumed to represent real values.



(a) Operational Amplifier

NOTE: The symbol Z can represent resistance or capacitive on inductive reactance.

(b) Potentiometric Amplifier

Figure A3.1 - Basic Amplifier Configurations

A3.1.1 Operational Mode, Figure A3.1(a)

The input signal applied to the operational configuration is e_i; the differential signal appearing across the amplifier input (summing junction (SJ) to ground) is ϵ, and the output voltage is e_o. The gain of the operational amplifier configuration is called the closed loop gain and is designated by $G = e_o/e_i$. The gain of the amplifier itself is called the open loop gain and is designated by $A = e_o/\epsilon$. Written in another form, the summing junction voltage is $\epsilon = e_o/A$. The open loop gain of the GPA-1 amplifier is approximately 10^6 and can be considered as approaching infinity. Therefore ϵ approaches 0. If the summing junction is considered to be 0 potential, the voltage drops across Z_i and Z_f are e_i and e_o, respectively. By Kirchoff's law, the sum of the currents entering and leaving the summing junction must equal 0. Since the input impedance of the amplifier is very high, little current flows through the input stage, and this current can be neglected (for simplification). Thus, the summation of current at the summing junction is $e_i/Z_i + e_o/Z_f = 0$. Rearranging terms, $e_o/e_i = -Z_f/Z_i = G$, which is the closed loop gain of the amplifier.

A3.1.2 Potentiometric Mode, Figure A3.1(b)

The symbols representing the voltages, impedances and gains are the same as that used in the operational amplifier. Similarly, as in the operational amplifier, ϵ approaches 0 as the open loop gain A approaches infinity. However, in the potentiometric mode, the summing junction voltage (SJ to ground) does not equal ϵ, but equals $\epsilon + e_i$. Since the total voltage applied across the feedback circuit is e_o, the summing voltage can be expressed as $e_o (Z_i/[Z_i + Z_f])$, or $\epsilon + e_i = e_o (Z_i/[Z_i + Z_f])$. Since ϵ approaches 0, it can be neglected. Rearranging terms, $e_o/e_i = 1 + Z_f/Z_i = G$, which is the closed loop gain of the amplifier.

A3.2 INPUT/OUTPUT CONSIDERATIONS

The primary function of a DC amplifier is to reproduce accurately the input signal on a linear scale fixed by the gain. External and internal circuit parameters can influence the desired output, unless provisions are made in the circuit design to compensate for these factors.

A3.2.1 Single-Ended/Differential Inputs

In the GPA-1 amplifier, the input signal e_i is defined as the difference between the input terminals. In the single-ended configuration (illustrated in figure A3.1), this definition is arbitrary, since the input signal is referenced to ground (established by convention). However, if the low side of the input is removed from ground (as in figure A3.2), the input configuration is differential and the difference between the

input terminals is referred to as the normal mode signal. Any signal common to both input terminals with respect to ground is called the common mode signal. Since this signal contains no useful information, it is discarded.

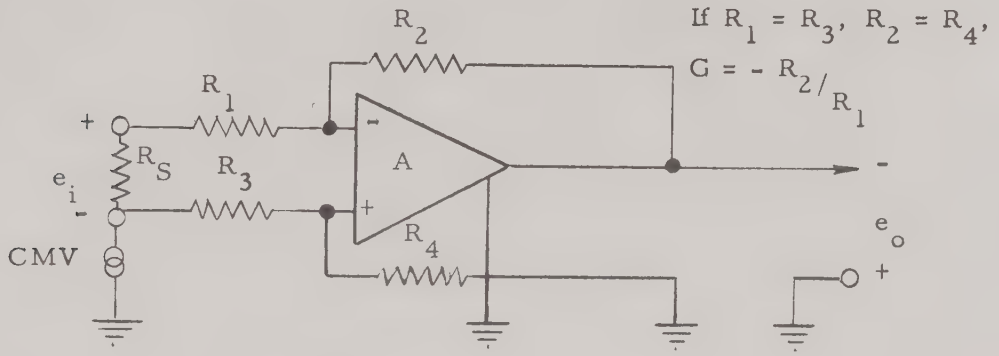


Figure A3.2 - Subtractor (Modified Operational Amplifier)

A3.2.2 Common Mode/Normal Mode

The GPA-1 amplifier exhibits high common mode rejection (approaching infinity), and if the common mode signal is actually common (identically the same) at both inputs, the signal will be eliminated in the amplifier. However, if the common mode signals are not the same at both inputs due to unequal voltage drops between the common mode source and the amplifier inputs, the difference across the inputs will add to the normal mode signal, creating an error. The amplifier cannot distinguish between the normal mode signal and this superimposed error and would amplify both signals if the error were not compensated for by some other means.

In the subtractor (balanced bridge) circuit shown in figure A3.2, the high and low sides of the input signal are applied across voltage dividers to ground. (The amplifier output impedance is very low and can be considered to be at ground for this discussion.) The source of common mode voltage is shown at the low side of the source resistance RS. As current flows in each divider, voltages are developed at the two amplifier inputs. If the dividers are adjusted so that $R_S + R_1 : R_2 = R_3 : R_4$, a voltage null is created at the amplifier input and the amplifier will see only the desired normal mode voltage. The circuit derives its name from the operation performed on the input signal, i.e. it subtracts the voltage of the low input from the high input and amplifies the difference.

A3.2.3 Input Bootstrapping

The GPA-1 has an auxiliary common mode (CM) terminal which can be used to drive an input shield at the common mode voltage. Consider for an example a voltage follower circuit illustrated in figure A3.3. This is a special type of potentiometric amplifier (see figure A3.1(b)), where $Z_i = \infty$ and $Z_f = 0$. By the gain formula, $G = 1 + 0/\infty$ or $G = 1$, and the output should be equal to the input. In addition, the output voltage should follow the input signal variations. In an ideal case, this would be true. However, in some installations, various impedances are present between the input signal line and ground (shown in dotted lines in figure A3.3). This may be due to the proximity of the signal wire to the chassis, or surrounding circuit elements. In either event, these impedances can result in a gain error if the signal source impedance is not zero.

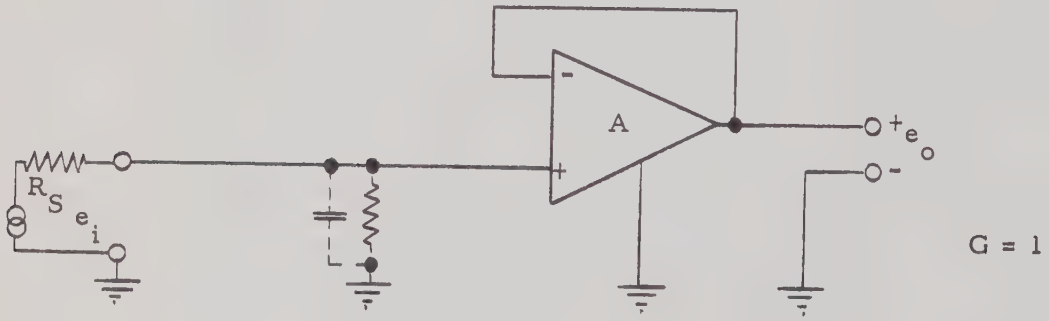


Figure A3.3 - Voltage Follower (Modified Potentiometric Amplifier)

Figure A3.4 shows a method of reducing the effect of signal to ground impedance. By surrounding the input signal line with a voltage equal to that line (driven by the amplifier), no current will flow through the signal to ground impedances and in effect, the signal line will ignore any impedance with respect to ground.

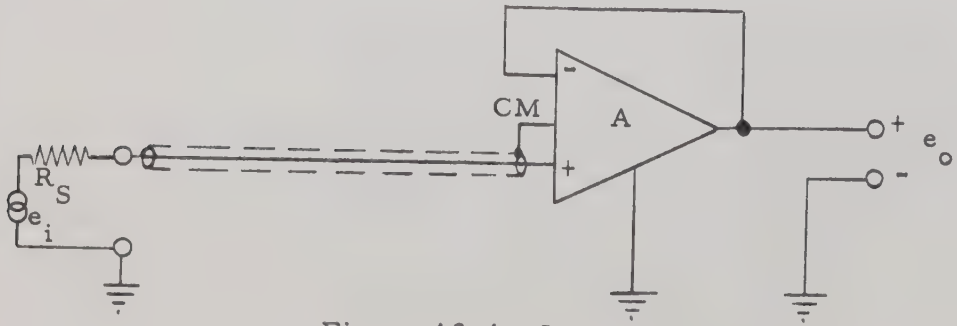


Figure A3.4 - Input Bootstrapping

A3.2.4 Four-Wire Output

In some applications, the resistance of the output signal lines can affect the accuracy of the amplifier. As shown in figure A3.5, the output current creates voltage drops across these resistances, subtracting from the true output (e_o) of the amplifier. This problem can be avoided by locating the output of the amplifier at the actual point of connection to the output load. In effect, this is accomplished by terminating the high side of the feedback loop and the signal low at the load (figure A3.6). These extended (sense) lines draw no load current and sample the output voltage at the load. Thus, the amplifier output is now defined at the point of contact with the load and any voltage drops in line resistances do not affect the overall performance of the amplifier.

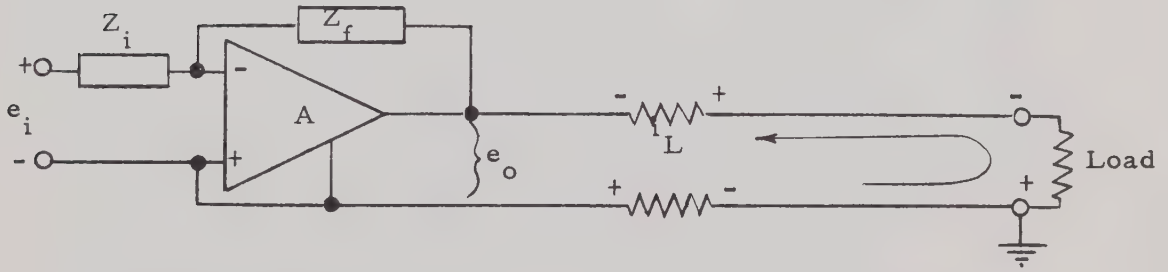


Figure A3.5 - Operational Amplifier (Showing Line Resistances)

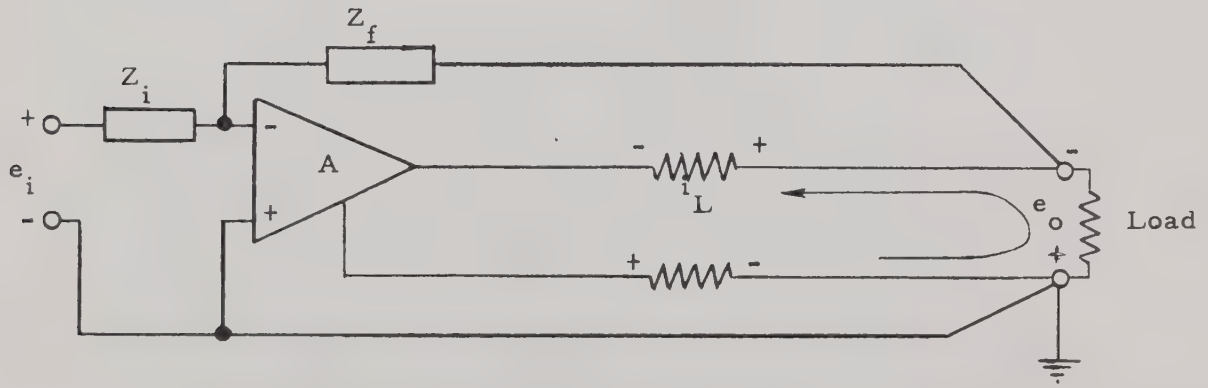


Figure A3.6 - Operational Amplifier (With Four-Wire Output)

A3.2.5 Integration

In certain applications, the amplifier configuration is designed to produce an output proportional to the integral of the input signal. A basic integrator circuit is shown in figure A3.7 with example (ideal) input and output waveforms. The slope and magnitude of the output signal e_o is determined by the RC time constant of the feedback loop by the formula shown. As in the basic operational amplifier (see paragraph A3.1.1) the current into the summing junction equals the current out. The current into the summing junction is $i = -e_i/R_1$ and the current out of the summing junction is $i = dq/dt = C\, de_o/dt$ (by Coulomb's Law). If the two current equations are solved simultaneously for e_o, $e_o = -1/RC \int e_i dt$.

An additional application of an integration type circuit is to attenuate noise superimposed on a DC signal. For this purpose, an operational amplifier with fixed gain determining resistances is used, and a capacitor is installed in parallel across the feedback resistance R_f. This type of circuit has two functions: to provide a fixed DC gain, and to integrate the superimposed noise. Since the integral (or average) of random noise is essentially zero, the circuit effectively attenuates the noise without affecting the DC voltage characteristics.

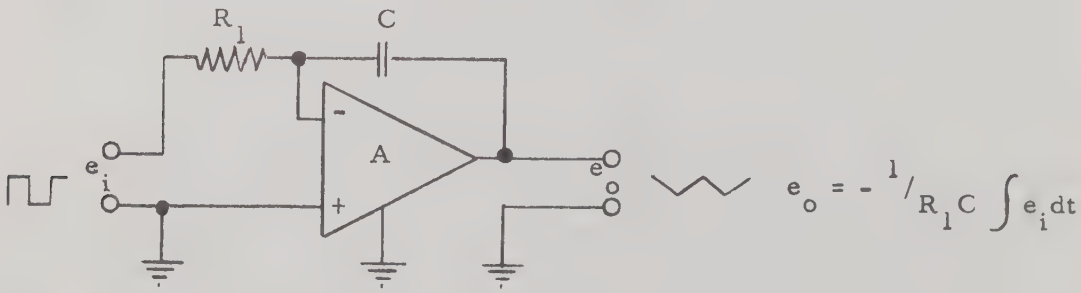


Figure A3.7 - Integrator

A3.3 CIRCUIT DESCRIPTION

For purposes of circuit description, the GPA-1 amplifier is broken down into four basic amplifier sections as shown in figure A3.8. K1 is the differential input amplifier, K2 is the output amplifier, K3 is the common mode amplifier, and K4 is the base current compensating amplifier. The common mode voltage (CMV) is herein defined as the average of the input voltages referred to common, and the normal mode voltage (NMV) is the difference between the inputs.

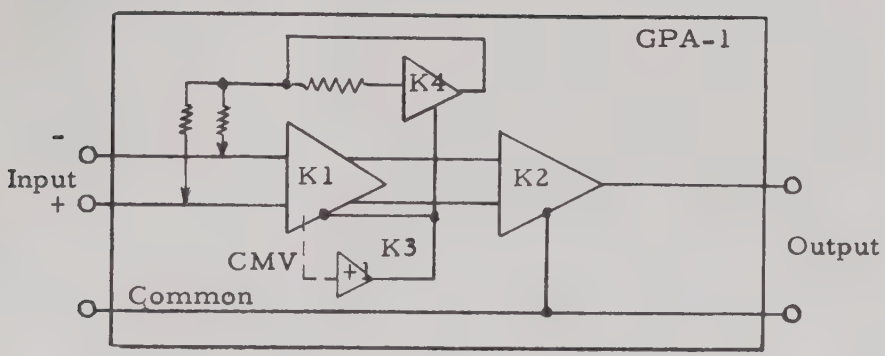


Figure A3. 8 - Simplified Diagram - Model GPA-1 General Purpose Amplifier

A3. 3. 1 General

Amplifier K1 has a differential input and a differential output. The output of amplifier K1 contains the CMV plus the amplified NMV. The entire amplifier K1, as well as amplifier K4, is driven at the CMV by the unity gain amplifier K3. Amplifier K2 attenuates the CMV while continuing to amplify the NMV. Amplifier K2 provides the necessary voltage and current excursions at the output.

A3. 3. 2 Amplifier K1

Amplifier K1 includes differential stages Q4, Q5 (Q9-Q10) and (Q14-Q15) which amplify NMV signals applied across the amplifier input (see schematic). All transistor terminals (emitter, base, collector) of these stages are driven at the CMV by the common mode amplifier K3 or are allowed to follow the common mode voltage by being returned to a supply through a current source. This results in very little of the CMV being converted into a NMV in these stages.

Resistors R16, R17, R25 and capacitors C10, C11, C3, C4 and C5 control the frequency response of the differential amplifier. Diodes CR2 and CR3 protect the input transistors from being damaged by overload.

A3. 3. 3 Amplifier K2

Amplifier K2 includes transistors Q16, Q17, Q18, Q19, Q20 and Q21. The amplifier receives the amplified NMV and the CMV (which has not been amplified) at the differential stage Q16 and Q17. Because the emitters of this stage are supplied with current by a constant current transistor Q18, this stage attenuates the CMV. The current changes developed in Q17 from the NMV are transferred to transistor Q22 which is sufficiently removed from the common (ground) level

to provide the necessary output voltage swing at the collector. Constant current transistor Q19 provides a return to the minus supply for the collector current of Q22. Transistor Q20 supplies load current out of the amplifier and transistor Q21 receives load current into the amplifier. Diodes CR9 and CR10 and resistors R51 and R52, in conjunction with the V_{be} drops of transistors Q20 and Q21, limit the maximum load current. Resistors R47 and R49 and capacitor C8 control the frequency response of the output amplifier.

Offset voltage originating in the input stages is cancelled by adjustment of potentiometer R27. Offset voltages outside the range of this potentiometer are accomodated by selection of resistor R26.

A3. 3. 4 Amplifier K3

Amplifier K3 consists of two emitter followers, transistors Q6 and Q8. The input of the amplifier is the CMV at the emitters of the input stage transistors, Q4A and Q4B. The output drives differential amplifier K1 and amplifier K4 at the CMV. The power supplied to amplifiers K1 and K4 comes from a voltage source and several current sources. The voltage source appears between the emitters of transistors Q11 and Q8. Zener diode CR6 receives its current from the constant current source, transistor Q12, and the current is buffered from the differential stages' load current by transistor Q11. Transistor Q7 provides a constant current for the input stages Q4 and Q5. Transistor Q13 maintains a constant current through differential stage Q9 and Q10.

A3. 3. 5 Amplifier K4

Amplifier K4 includes transistors Q1, Q2 and Q3, and provides temperature compensated base currents to the input stage. These currents cancel the offset currents and are supplied through potentiometers R6 and R7 and resistors R9 and R10.

A3. 3. 6 Constant Current Supplies

The GPA-1 amplifier does not require regulated voltage supplies. The amplifier has a built-in insensitivity to supply voltage ripple or slow voltage variations. Zener diode CR5 supplies a constant voltage for constant current transistors Q7, Q13, Q18 and Q19. Since the voltage across the emitter resistors of these transistors (the Zener voltage minus the V_{be} of the transistor) is constant even with line variations, the current through the transistors will also be constant. Zener diode CR8, in conjunction with resistors R37 and R38 and diode CR7, maintains a constant voltage across resistor R36. This forces transistor Q12 to provide a constant collector current.

SECTION IV
CALIBRATION

A4.1 GENERAL

The calibration procedure should be performed prior to the test procedure outlined in paragraph A5.3 and subsequent to any corrective maintenance. Calibration of the Model GPA-1 amplifier consists of adjusting three trimpots for proper DC balance (paragraph A4.4). To perform the calibration procedure, the amplifier must be removed from associated circuitry and be checked under controlled conditions. The operating conditions for the calibration and test procedures are controlled by a special test fixture. The test fixture can be built in the field (using standard components), or can be obtained from Electro Instruments, available on special order. A schematic diagram for an improvised test fixture is illustrated in figure A4.1.

NOTE

For field installations not requiring rigid tolerance specifications, a modified test fixture providing for a less rigorous calibration procedure is described in paragraph A4.5.

A4.2 CONSTRUCTION OF TEST FIXTURE

It should be possible to obtain all parts for the improvised test fixture from a local distributor. Construction details are outlined below:

1. Use a metal chassis for maximum shielding.
2. Mount the power transformer greater than 10" from the plug-in receptacle.
3. Mount switches $+R_i$ and $-R_i$ close to the plug-in receptacle.
4. Mount all switch parameter resistors on switches.
5. Install a shield plate behind the front panel switches.
6. Keep all leads as short as possible.
7. Common leads should be size No. 22 or greater.
8. Tie all common leads to one common point near pin 7 of the plug-in receptacle terminal strip.
9. All voltage leads should be as far removed from terminal strip as possible.

LEGEND

T1: Triad F90X or equivalent
M1: ±50 microamps full scale from center zero, 1 kilohm meter movement, (different resistance value can be used with appropriate multiplier resistors)
CR1 and CR2: 10 to 12V Zener diodes
Plug-in Receptacle (Circled Pin Numbers): Cinch 250-12-30-170 or equivalent

Resistors are carbon, 1/4 watt, 5% except where otherwise specified.
Capacitors should have 20% tolerance; in power supply the capacitors should have a voltage rating of 50V or more.
Diodes are standard silicon type; in power supply the diodes should have a voltage rating of 50V or more.

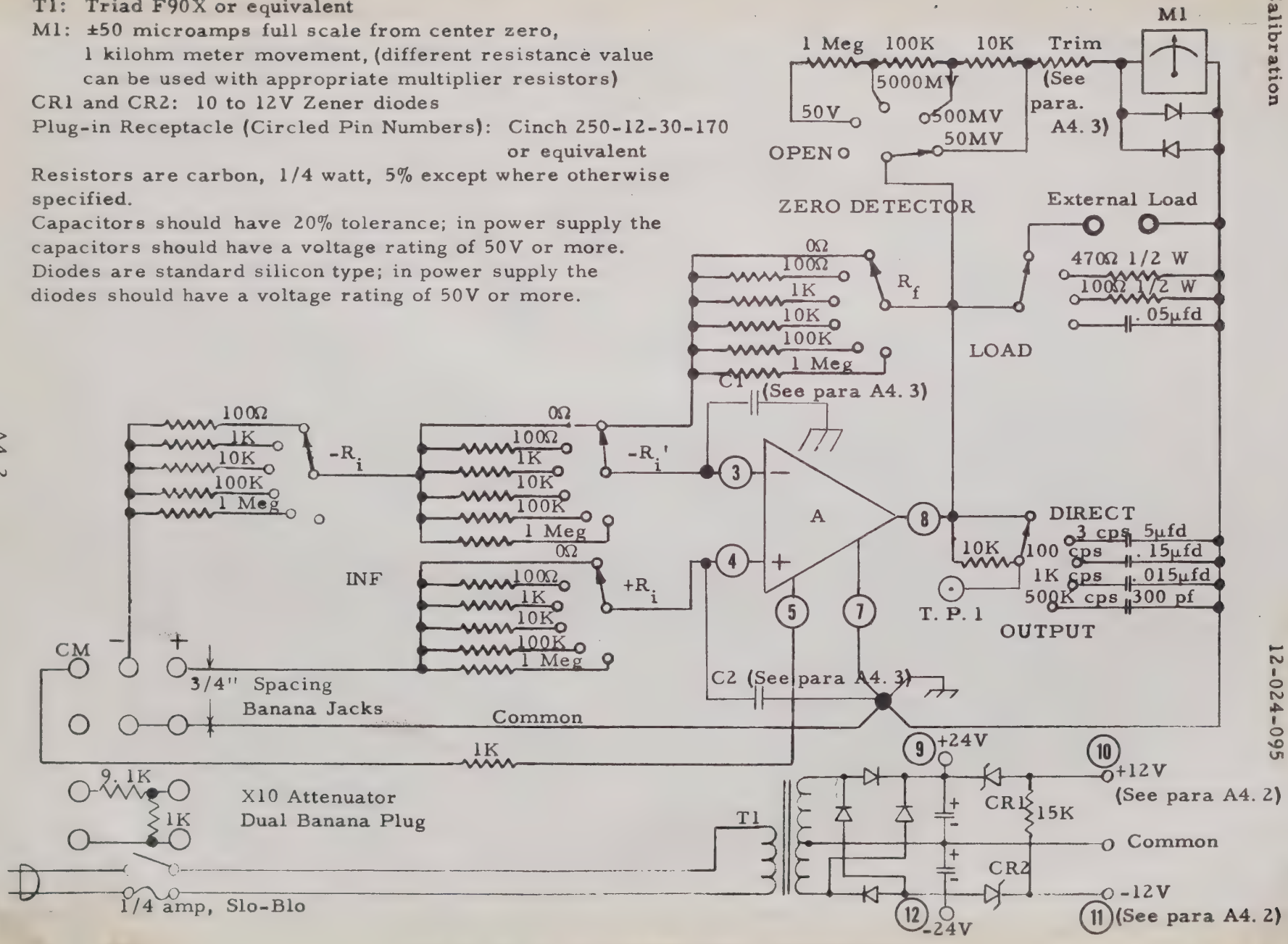


Figure A4. 1 - Improved GPA-1 Test Fixture

10. Banana jack connectors should be vertically spaced by 3/4". This allows for the use of dual banana plug connectors.

11. If jumpers 2 and 3 on the amplifier board are installed, the + and - 12V supplies should not be connected to the amplifier (terminals 10 and 11).

12. Provision should be made for shielding the amplifier from air currents, when plugged into the receptacle. This can be accomplished by means of a metal shield, or a cloth draped over the amplifier board.

A4.3 CALIBRATION OF TEST FIXTURE

When the test fixture has been completely assembled, insert an amplifier board into the plug-in receptacle. Calibration instructions are outlined below:

a. Set front panel controls as follows:

$+R_i$	0
$-R_i$	100Ω
$-R_i$	0Ω
R_f	100K
OUTPUT	DIRECT
ZERO DETECTOR	OPEN
LOAD	470Ω

b. Connect shorting plugs from + and - input terminals to common.

c. Apply AC power to the fixture and turn power on.

d. Connect a VTVM between T. P. 1 and common.

e. Set the voltage offset adjustment on the amplifier (see figure A4.2) for an offset of 50 millivolts, as monitored on the VTVM.

f. Set $-R_i'$ to successively higher resistance values while observing the VTVM. Then set $-R_i'$ to 0 and repeat the procedure for $+R_i$. If the amplifier is unstable when switching $-R_i'$ and $+R_i$ to high resistances, stabilization capacitors C1 and C2 should be added from the amplifier terminals 3 and 4 to common. Values can range from 100 pf to .001μfd.

g. At this point, meter M1 should read 0. If not, set the meter centering adjustment for a zero reading.

h. Set $+R_i$ to 0Ω, R_f to 100K and $-R_i'$ to 100Ω. Check that the output of the amplifier is 50 millivolts.

Figure A4.2 - GPA-1 Printed Circuit Board

i. Set the LOAD switch to External Load and the ZERO DETECTOR switch to 50MV. Connect a jumper across the points labeled "trim" in figure A4. 1. If a meter with an internal resistance of 1K was used, the meter should read +50 millivolts. If the meter does not read 50 millivolts, use a resistor substitution box in place of the jumper to determine the value of the trim resistor required. Install a trim resistor and check that the meter reads 50 millivolts.

A4. 4 OFFSET ADJUSTMENTS

The calibration procedure for the amplifier offset adjustments is outlined below. If the amplifier cannot be calibrated, refer to paragraph A5. 5

a Set front panel controls as follows:

$+R_i$	0Ω
$-R_i$	100Ω
$-R_i'$	0Ω
R_f	100K
OUTPUT	DIRECT
ZERO DETECTOR	OPEN
LOAD	External Load

b. Connect shorting plugs from + and - input terminals to common. Plug amplifier board into fixture and turn power on. Allow 15 minutes warmup time.

c. Set the ZERO DETECTOR switch to the 50MV position. Set the voltage offset adjustment R27 on the amplifier (figure A4. 2) for a meter deflection with ±2 millivolts.

d. Set the negative input current offset adjustment R7 for minimum zero meter deflection while switching $-R_i'$ from 0Ω to 100K. Return $-R_i'$ to 0Ω.

e. Set the positive input current offset adjustment R6 for minimum zero meter deflection while switching $+R_i$ from 0Ω to 100K. Return $+R_i$ to 0Ω.

f. Recheck the meter deflection for ±2 divisions of zero. If necessary, set the voltage offset adjustment R27 for ±2 millivolts on the meter. Return the ZERO DETECTOR switch to the OPEN position.

A4.5 ALTERNATE CALIBRATION PROCEDURE

An alternate test fixture is illustrated in figure A4.3. The setup does not provide for all of the maintenance checks outlined in section V, however it does allow for adjustment of the calibration potentiometers on the GPA-1 assembly board. A precision 5-digit digital voltmeter with an accuracy of .01% or better should be used to monitor the output voltage of the amplifier - test fixture configuration. The procedure is outlined below:

a. Close S1 and S2. Set the Voltage Offset Adjustment (figure A4.2) for an output of less than 10 mv, as monitored on the digital voltmeter. Note this level as the zero reference.

b. Open S1. Set the Positive Input Current Offset Adjustment to the zero reference level noted in step a above.

c. Close S1 and open S2. Set the Negative Current Offset Adjustment to the zero reference level noted in step a.

d. Recheck steps a, b and c above.

SECTION V

MAINTENANCE

A5.1 GENERAL

The Model GPA-1 requires no periodic maintenance. The amplifier can be operated continuously without any adverse effect on its life. If a malfunction is evident, first calibrate the amplifier as outlined in paragraph A4.4. If the amplifier cannot be calibrated, i.e. if the offset adjustments do not provide sufficient range to correct the offsets, refer to paragraph A5.5. After the amplifier is properly calibrated, perform the test procedure outlined below. Performance of these checks will either (1) verify that the amplifier is operating within allowable tolerances, or (2) help isolate the malfunction as an aid to trouble analysis. In the first case, the amplifier should be returned to the circuit from which it came. If a malfunction continues to exist, the surrounding circuitry is at fault. In the second case, corrective maintenance should be performed as outlined in paragraph A5.4.

A5.2 TEST EQUIPMENT REQUIRED

a. GPA-1 Test Fixture

b. VTVM

c. Oscilloscope with a DC sensitivity of at least 1 mv/cm.

d. Sine wave generator, 100 cps minimum to 500KC, at least 25 volts peak-to-peak output, and a maximum output impedance of 1K, such as a Hewlett-Packard Model 200CD.

e. X10 attenuator dual banana plug (see figure A4.1).

A5.3 TEST PROCEDURE

a. Set front panel controls of test fixture as follows:

$+R_i$	0Ω
$-R_i$	10K
$-R_i'$	0Ω
R_f	100K
OUTPUT	DIRECT
ZERO DETECTOR	OPEN
LOAD	470Ω

b. Plug amplifier board into test fixture and turn power on. Allow 15 minutes warmup time. Connect oscilloscope from T.P. 1 on the fixture to common. Monitor all steps.

c. Connect the generator from the - input terminal to ground. The + input terminal should be shorted to ground.

d. Set the generator for a frequency of 5KC. Set the generator output voltage for 24V P/P. The sine wave peaks should not be clipped.

e. Change the generator frequency to 100 cps. Set the LOAD switch to 100Ω. Increase the generator output until the amplifier output clips. The peak amplitude should be between 2 volts and 3.5 volts.

f. Change the generator frequency to 1KC. Set the LOAD switch to .05 mfd. Increase the generator output to an amplifier overload condition and return. The amplifier should recover. Return the LOAD switch to External Load.

g. Set the front panel controls of the test fixture as follows:

$+R_i$	0Ω
$-R_i$	1NF
$-R_i$,	0Ω
R_f	0Ω
OUTPUT	DIRECT
ZERO DETECTOR	OPEN
LOAD	External Load

h. Connect the X10 attenuator dual banana plug between the + input terminal and common.

i. Connect the generator from the + input terminal of the dual banana plug connector to common. Set the frequency for 1KC.

j. Set the oscilloscope for a sensitivity of .01V/cm and AC coupling.

k. Adjust the generator for an amplitude of .03V P/P appearing at the output of the amplifier.

l. Center the signal waveform to the center of the scope face. Increase the generator frequency while monitoring the amplifier output. There may be an increase in amplitude between 100KC and 500KC. The signal should not exceed .04V P/P. At 500KC the wave shape should not be distorted and the amplitude should not decrese below .02V P/P of the 1KC setting.

A5.4 CORRECTIVE MAINTENANCE

If the amplifier does not respond properly to the test procedure, the following steps should be followed:

a. Remove the board from the test fixture and check for solder shorts across the printed circuit straps.

b. Re-insert the board in the test fixture and set the front panel controls as follows:

$+R_i$	0Ω
$-R_i$	1NF
$-R_i'$	0Ω
R_f	0Ω
LOAD	External Load

c. Connect shorting plugs from + and - input terminals to common.

d. The amplifier is now set up in a condition from which the voltage levels appearing on the schematic were taken. Check the voltages on the amplifier board against the voltages shown on the schematic. Refer to paragraph A3. 3 for circuit description and use standard troubleshooting techniques to locate the malfunction. Since each amplifier is tested and calibrated prior to shipment, the following assumptions should be made in troubleshooting:

1. The amplifier is wired correctly.
2. Transistor troubles are usually limited to: open, short, and noisy.
3. Diode failures are: open and shorted.
4. Resistors become open or increase in value.
5. Capacitors can be open or shorted.

e. When a faulty component is found, use an exact replacement or equivalent part. If a single transistor of a matched pair is bad, replace both transistors with a matched pair. If any component is changed, repeat the calibration procedure.

A5. 5 REPLACEMENT OF TRIM RESISTORS

Trim resistors are selected at the factory and normally do not require replacement. However, if the offset adjustments do not provide sufficient range to calibrate the instrument (paragraph A4. 4), or if transistor Q1, Q4 or Q5 is replaced or the associated circuit otherwise misaligned, it may be necessary to replace one or both trim resistors. The procedure for selection of trim resistors is outlined below.

A5. 5. 1 Current Offset Trim Resistor R3'

a. Set the voltage offset adjustment R27 to mid-position (12-1/2 turns from end stop).

b. Set front panel controls of test fixture as follows:

$+R_i$	0Ω
$-R_i$	1NF
$-R_i'$	0Ω
R_f	0Ω
OUTPUT	DIRECT
ZERO DETECTOR	OPEN
LOAD	External Load

c. Connect shorting plugs from + and - input terminals to common. Plug amplifier board into fixture and turn power on. Allow 15 minutes warmup time.

d. Connect the VTVM from the amplifier board test pin to common. If the test point voltage is between +.75V and +.90V, it will not be necessary to replace R3'. It will be necessary to replace the trim resistor R3' only if the test point voltage is less then +.75V or greater than +.90V.

e. If the test point voltage is out of the limits described in step d, remove R3' from the amplifier board and solder a temporary jumper across the points of connection for R3'. (See figure A4.2.)

f. Refer to table A5.1. The voltage at the test point subtracted from +.8V is the E_1-E_2 value and should be used to select resistor R3' from the table. The closest stock value should be installed on the board. Replacement resistor should be 1/4 watt, composition, 5% tolerance.

g. If the initial voltage happens to be above +.8 volts, the 10 megohm resistor R3 should be replaced with a 5.6 megohm resistor. The formula for finding R3' is:

$$\frac{(E_1 - E_2)\, R_3}{E_2}$$

E_1 = +.8 volts
E_2 = measured voltage appearing at test pin
R_3 = 10 megohm or 5.6 megohm

h. After the trim resistor is installed, recheck the voltage at the test point. The allowable limits are between +.75 volts and +.90 volts.

Table A5. 1 - Selection of R3' (R3 = 10 megohm)

$E_1 - E_2$	R_3'
.1 Volt	1.5 megohm
.15 Volts	2.4 megohm
.20 Volts	3.3 megohm
.25 Volts	4.7 megohm
.30 Volts	6.2 megohm
.35 Volts	7.5 megohm
.40 Volts	10.0 megohm
.45 Volts	12.0 megohm
.50 Volts	15.0 megohm

A5. 5. 2 Voltage Offset Trim Resistor R26

a. Set front panel controls of test fixture as follows:

$+R_i$	0Ω
$-R_i$	100Ω
$-R_i'$	0Ω
R_f	100K
OUTPUT	DIRECT
ZERO DETECTOR	OPEN
LOAD	External Load

b. Set the ZERO DETECTOR switch to successively lower resistance positions until the meter deflection is mid scale or greater. Since the amplifier is set up for a gain of X1000, the amount of voltage offset is determined by the meter reading in millivolts divided by 1000. This is the same as reading the voltage offset directly in microvolts.

c. If the ZERO DETECTOR switch is now in the 50MV or 500MV positions and the meter reads less than full scale, repeat the calibration procedure (paragraph A4. 4). If the meter reads full scale or greater, or if the ZERO DETECTOR switch is in another position, remove the current offset trim resistor R26 from the amplifier board.

d. Refer to table A5. 2 and select the trim resistor corresponding to the measured offset. The replacement resistor should be an eighth-watt, metal film type, 1% tolerance, T8 or T9 temperature coefficient (RN60E)

Table A5.2 - Selection of R26

Measured Offset	R26
0μv to ± 500μv	NONE
±500μv to ±1000μv	249K
±1000μv to ±1500μv	124K
±1500μv to ±2000μv	88.5K
±2000μv to ±2500μv	61.9K
±2500μv to ±3000μv	49.9K
±3000μv to ±3500μv	41.2K

e. Refer to figure A5.1. If the offset is positive, the select resistor is installed across area No. 1. If the offset is negative, the select resistor is installed across area No. 2.

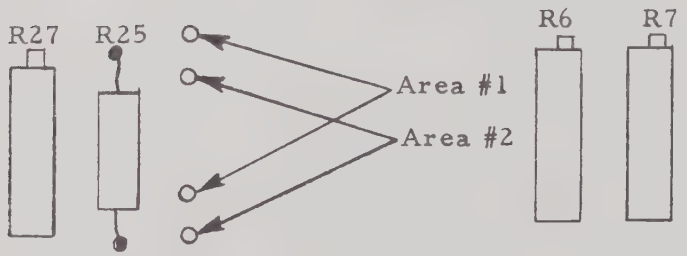


Figure A5.1 - Location of Trim Resistor R26

f. Repeat the calibration procedure (paragraph A4.4).

LOGIC AND SYMBOLOGY FOR DIGITAL INSTRUMENTS

INTRODUCTION

This manual has been prepared by Honeywell Inc., as an introduction to the type of logic circuitry normally used in their digital instruments. It is primarily intended as a training and familiarization aid for those concerned with operating and servicing Honeywell equipment in the field.

The logic described applies to digital instruments, but does not necessarily apply to the entire range of Honeywell products.

PARTS LIST

INTRODUCTION

The parts list is a breakdown of all assemblies and sub-assemblies which can be disassembled. Generally parts are listed in order of disassembly sequence.

COLUMN EXPLANATIONS

a. References

This is a triple column which lists first, the figure number of the illustration on which a particular index number will be found. The second column contains the index number of the item described. The third column lists the schematic reference designation of an electrical component.

b. Description

The item name appears in this column. Where applicable the specification number, value and/or reference which further identifies the item is also listed.

c. Manufacturer and Part Number

This is a double column which lists first the manufacturer's Federal Supply Code. This is a five digit code as described in the Federal Supply Code for Manufacturers (Cataloging Handbook H4-1 & H4-2.) A letter code is assigned to manufacturers who do not have a Federal Supply Code Number. In some cases more than one manufacturer can supply an "or equal" part, but the intent is to show only one outside source. The second column lists the manufacturer's part number for all parts that may be ordered directly from the original manufacturer.

d. Honeywell Part Number

This column lists the number under which an item may be ordered directly from Honeywell Inc., Test Instruments Division, San Diego. Certain items contain only Honeywell part numbers. These items are proprietary items that are available only from Honeywell.

e. Quantity per Assembly

This column lists a number which is the quantity of that item as used in a particular assembly.

REFERENCE DESIGNATORS

The following lists the abbreviations used with schematic reference designators:

B	-	motor	NR	-	Nixie tubes
C	-	capacitor	P	-	plug
CR	-	diode	Q	-	transistor
DS	-	device signaling (lamp)	R	-	resistor
F	-	fuse	RT	-	thermistor
FL	-	filter	S	-	switch
J	-	jack	T	-	transformer
K	-	relay	TP	-	test point
L	-	inductor	V	-	vacuum tube
M	-	meter			

ABBREVIATIONS

The following abbreviations are used in the "Description" column of the parts list:

AC	-	alternating current	BRKT	-	bracket
AMP	-	ampere	CAP	-	capacitor
ARM	-	armature	CRT	-	cathode ray tube
ASSY	-	assembly	CER	-	ceramic
BAT	-	battery	COMP	-	composition
BLK	-	black	CONN	-	connector
BLO	-	blower	DIA	-	diameter
BOT	-	bottom	DC	-	direct current

VDC	-	direct current volts	MEG	-	megohm
DIO	-	diode	METFLM	-	metal film
DP	-	double pole	METMY	-	metallic mylar
DPDT	-	double pole double throw	NHA	-	next higher assembly
DPST	-	double pole single throw	NO	-	number
DT	-	double throw	Ω	-	ohm
ELECT	-	electrolytic	ORN	-	orange
FIG	-	figure	POLY	-	polystyrene
FIL H	-	fillister head	POT	-	potentiometer
FXD	-	fixed	RES	-	resistor
4P	-	four pole	SP	-	single pole
GL	-	glass	SPDT	-	single pole double throw
GRN	-	green	SPEC	-	specification
GROM	-	grommet	SPST	-	single pole single throw
H	-	henry	SOT	-	value select on test
HEX	-	hexagon	SEMICON	-	semiconductor
IN	-	inches	Si	-	Silicon
K	-	kilohm	Ta	-	tantalum
L	-	left	TGL	-	toggle
μF	-	microfarad	V	-	volt
μμF	-	micromicrofarad	W	-	watts
MTG	-	mounting	WW	-	wirewound

MANUFACTURER

Following is the list of manufacturers which appear in the parts list. The Federal Supply Code is listed in numerical order and corresponding manufacturer's name and address is given.

LIST OF MANUFACTURERS

MODEL EI-85

00116 Honeywell Inc.
Test Instruments Div.
8611 Balboa Ave.
San Diego, Calif. 92112

00779 Amp. Inc.
Eisenhower Blvd.
Harrisburg, Pa.

01121 Allen Bradley Co.
1201 S. 2nd St.
Milwaukee, Wisconsin

02816 Dialco
60 Stewart Ave.
Brooklyn, New York

03615	Ohmite Mfg. Co. 6115 Selma Ave. Hollywood, Calif.
04062	El Menco Arco Electronics Inc. Community Dr. Great Neck, New York
04202	Winchester Electronic Div. Litton Inc. Main St. & Hillside Ave. Oakville, Conn.
04713	Motorola Semiconductor Products Inc. Box 955 Phoenix, Arizona
05267	Pomona Electronic 1500 E. 9th Street Box 2767 Pomona, Calif.
06136	Ward Leonard Electric Co. 23 South St. Mount Vernon, New York
06228	Texas Instrument Inc. Box 5474 Dallas, Texas
06540	Amatom Electronic Hard- ware Co., Inc. 432 Main St. Bristol, Conn.
06751	Semcor Div. Components Inc. 3540 W. Osborn Rd. Phoenix, Arizona
07115	Corning Glass Works Elctn. Products Div. 3901 Electronics Drive Raleigh, North Carolina
07263	Fairchild Semiconductor Corp. 313 Fairchild Drive Mountain View, Calif.
07910	Continental Device Corp. 12515 Chadron Ave. Hawthorne, Calif.
09026	Babcock Relays Div. Babcock Elctrns. 3501 Harbor Blvd. Box 1499 Costa Mesa, Calif.
09213	General Electric Co. Semiconductor Products Dept. of Electronic Components Div. of Electronic, Atomic & Defense System Groups Buffalo, New York
12406	Elpac Inc. 4270 Artesia Fullerton, Calif.
14936	General Instrument Corp. Semiconductor Product Grp. 600 W. John St. Hicksville, New York
15636	Elec-Trol Inc. 18828 Bryant St. Northridge, Calif.
16037	Spruce Pine Mica Co. Spruce Pine, North Carolina
21604	Buckeye Stamping Co. 555 Marion Rd. Columbus, Ohio
24655	General Radio 22 Baker Ave. W. Concord, Mass.

37942 Mallory & Co. Inc.
3029 E. Washington St.
Indianapolis, Indiana

49671 Radio Corp. of America
Electronics Components
Devices
415 S. 5th St.
Harrison, New Jersey

56289 Sprague Electric Co.
125 Marshall St.
North Adams, Mass.

70903 Belden Mfg. Co.
415 S. Kilpatrick Ave.
Chicago, Illinois

71590 Centralab
Div. Globe-Union Inc.
Box 591
Milwaukee, Wisconsin

71785 Cinch Jones Mfg. Co.
1026 Homan Avenue
Chicago, Illinois

72653 General Cement
Div. of Textron Inc.
Rockford, Illinois

73293 Hughes Aircraft Co.
Semiconductor Div.
500 Superior Avenue
Newport Beach, Calif.

73734 Federal Screw Products Inc.
3917 N. Kedzie Ave.
Chicago, Illinois

73899 JFD Electronics Corp.
Components Div.
15th Ave. at 62nd St.
Brooklyn, New York

74970 E. F. Johnson
1923 10th Avenue
S. W. Weseca, Minn.

75042 International Resistance Co.
414 North 13th St.
Philadelphia, Pa.

75915 Littelfuse Inc.
800 E. Northwest Hwy.
Des Plaines, Illinois

80294 Bourns Inc.
Trimpot Div.
1200 Columbia Ave.
Riverside, Calif.

81074 Holub Ind. Inc.
468 Elm St.
Sycamore, Illinois

81483 International Rectifier Corp.
233 Kansas St.
El Segundo, Calif.

82768 Phillips Advance Controls
59 W. Washington
Joliet, Illinois

82867 Rotron Mfg. Co. Inc.
Hasbrouck Lane
Woodstock, New York

83125 Pyramid Electric Co.
507 26th Street
Union City, New Jersey

83330 Herman H. Smith Inc.
812 Snediker Avenue
Brooklyn, New York

83594 Burroughs Corp.
Electronics Components Div.
Box 1226
Plainfield, New Jersey

87216	Philco Corp. Lansdale Div. Micro-electronics Oper. Church Road Lansdale, Pa.
87930	Tower Mfg. Corp. 158 Pine St. Providence, R. I.
88245	USECO Div. Litton Inc. 13536 Salicoy St. Van Nuys, Calif.
94271	Weston Instruments Inc. Weston Archbald Div. Archbald, Pa.
99515	Electron Products Div. of Marshall Ind. 1960 Walker Avenue Monrovia, Calif.
A1000	Wheelock Signals, Inc. 273 Branchport Ave. Long Beach, New Jersey
A2000	Transformer Engineers 1039 E. Valley Blvd. San Gabriel, Calif.
A3000	Lemo Div. 150 California St. San Francisco, Calif.

ORDERING INFORMATION

When ordering spare or replacement parts address your order or inquiry either to a Honeywell sales representative nearest you or to:

CUSTOMER SERVICE
HONEYWELL, INC.
TEST INSTRUMENTS DIVISION
8611 BALBOA AVENUE
SAN DIEGO, CALIF. 92112

When ordering, always include the following information:

a. Model and serial number of instrument.

b. Honeywell part number.

c. Description.

d. If applicable, the reference designator.

PARTS LIST

The following lists all parts, less standard hardware. Parts that are subject to electrical or mechanical damage on an isolated or individual basis are listed.

The parts list uses a system of column indentation to show the relationship between the various items.

REFERENCES FIG	REFERENCES IND	REFERENCES SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			MODEL EI-85 DIGITAL MULTIMETER					
			Board Extender					
			Board extenders may be used to extend the plug-in circuit boards for easy access to components and test points under operating conditions. These boards may be purchased from Honeywell.					
			. Board Extender	00116		105-124-84		
			. Top Cover Assy	00116		115-397-81	1	
			. . Top Cover	00116		115-397-30	1	
			. . Inner Cover	00116		115-399-30	1	
			. . Barrier Strip	00116		105-346-31	3	
			. . Barrier Strip	00116		115-402-30	1	
			. . Spacer Bar	00116		105-325-33	1	
			. . Spacer Bar	00116		105-343-32	1	
			. Rack Mtg. Angle	00116		115-453-30	2	
			. Chassis Assy	00116		115-410-82	1	
			. . Bottom Cover	00116		115-398-30	1	
			. . Rail, left side	00116		115-314-31	1	
		T1	. . Transformer	00116		96-43-031	1	
			. . Rail, right side	00116		115-309-33	1	
			. . . Receptacle Mtg. Block	00116		115-320-32	1	
			. . Bottom Spacer	00116		105-326-33	1	
			. . Bottom Spacer	00116		105-344-32	1	
			. . Barrier Strip	00116		105-356-31	3	
			. . Barrier Strip	00116		115-401-30	1	
			. . Standoff	00116		104-415-30	2	
			. . Cable Clamp, 1/4"	81074	EC-5	74-11-005	3	
			. . Conn. Mtg. Bar Spacer, upper	00116		105-325-33	1	
			. . Conn. Mtg. Bar Spacer, lower	00116		105-326-33	1	
			. . Conn. Mtg. Bar	00116		105-328-33	2	
		J1 thru J5	. . Connector, 62 pin	04202	PQ-62A	70-90-660	5	
			Schematic (reference)	00116		115-116		

REFERENCES FIG	REFERENCES IND	REFERENCES SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Rear Rail Assy	00116		105-386-87	1	
			. . Rear Rail	00116		115-376-35	1	
			. . Fuseholder	75915	342003	72-05-050	2	
		F1, F2	. . Fuse, 2 amp. Slo-Blo	75915	313002	72-02-045	2	
		J101,J102,J103	. . Connector, 50 pin	00779	202215-2	70-04-022	3	
			. (Mating Connector)	00779	202214-2	70-04-020		
		J104	. . Connector, 3 pin	87930	H-106-11G-3L	70-70-001	1	
			. . Fan, Muffin Venturi	82876		41-20-050	1	
			. Input Cable	05627	2077	98-28-116	2	
			. Power Cord	70903	KH4147	98-28-108	1	
			. Front Panel	00116		115-478-30	1	
			. Knob. Control	21604	PS-95-CL-2	70-02-028	2	
			. Knob, Control	21604	PS70DL-2	70-02-016	2	
			. Knob, Control	21604	PS-70-1	70-02-013	1	
			. Knob, Control	21604	PS-70DL-1	70-02-014	1	
			. Anti-Reflection Window	00116		00-50-022	1	
			. Long Card Number Decal	00116		008-001-30	1	
			. Sub Panel Assy	00116		115-404-82	1	
			. . Sub Panel	00116		115-404-32	1	
			. . Bezel Assy	00116		00-50-083B	1	
			. . Bezel	00116		115-438-30	1	
			. . Hinge	00116		115-455-30	2	
			. . Detent Block	00116		105-303-32	2	
			. . Standoff	00116		105-304-31	4	
		DS-MV, DS6	. . Indicator Light, white lens	02816	249-9540-XP13-1435	75-05-008	2	
		S1	. . Switch, Power 2 Pol. 2 Pos. spec. no. 010-523-00	00116		95-80-381	1	
			. Readout Plate Group Assy	00116		105-383-81	1	
		DS1 thru DS5	. . Indicator Light, white lens	02816	249-9540-XP13-1435	75-05-008	5	
			. Readout Plate Assy	00116		105-390-81	1	
			. . Socket, 13 pin	83594	SK-112	73-75-030	6	
		NRS	. . Nixie Tube, symbol	83594	B6032	75-10-010	1	
		NR1 thru NR5	. . Nixie Tube, number	83594	B6091	75-10-018	5	
			. . Front Door, Inner	00116		105-336-35	1	
			. . Shield	00116		105-377-36	1	
			. . Shield	00116		105-441-32	1	
			. . Resistor, fxd. WW 250Ω 5W .5%	06136	5XM250	87-54-307	1	
			Schematic (reference)	00116		115-116		

REFERENCES FIG	REFERENCES IND	REFERENCES SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Outside Power Supply & Control Logic Board Assy	00116		115-121-84	1	
			. . Handle	00116		00-36-024B	1	
		C1 thru C7, C10	. . Capacitor, fxd. elect. 100μF 25V	56289	30D188A1	61-04-107	8	
		C11, C12	. . Capacitor, fxd. elect. 16μF 350V	83125	TD-16-350	61-70-166	2	
		C13	. . Capacitor, fxd. metmy. 1μF 200V	12406	ZX2A-105K	55-00-105	1	
		C14, C15	. . Capacitor, fxd. cer. 47μμF 1000V	71590	DD-470	48-10-471	2	
		C16, C23	. . Capacitor, fxd. elect. 50μF 15V	56289	40D168A2	61-11-506	2	
		C17, C19, C21	. . Capacitor, fxd. metmy. .15μF 200V	12406	ZX2A-154K	55-00-154	3	
		C18, C20, C24 C30	. . Capacitor, fxd. metmy. .01μF 200V	12406	ZX2A-103K	55-00-103	4	
		C22	. . Capacitor, fxd. elect. 200μF 15V	56289	30D174A1	61-03-207	1	
		C24, C26	. . Capacitor, fxd. cer. 220μμF 50V	56289	40C204A	45-05-221	2	
		C25, C27, C28	. . Capacitor, fxd. cer. 560μμF 1000V	71590	DD-561	48-10-561	3	
		C29	. . Capacitor, fxd. metmy. .22μF 200V	12406	ZX2A-224K	55-00-224	1	
		CR1 thru CR4 CR6 thru CR9 CR35 thru CR38	. . Semicon. Device, Diode spec. no. 43235	00116		94-43-235	12	
		CR5, CR34	. . Semicon. Device, Diode	04713	1N965B	92-09-655	2	
		CR10, CR12 thru CR27, CR29 thru CR33, CR40 CR41	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	24	
		CR28	. . Semicon. Device, Diode	07910	1N967A	92-09-672	1	
		Q1, Q2	. . Transistor, Germanium PNP	49671	2N1183A	91-11-833	2	
		Q3, Q4, Q21	. . Transistor, Germanium NPN	06228	2N1304	91-13-040	3	
		Q5, Q7, Q8, Q10, Q11, Q13, Q14, Q15, Q16, Q19	. . Transistor, Germanium PNP	09215	2N404A	91-04-043	10	
		Q6, Q9, Q12	. . Transistor, Germanium PNP	49671	2N1384	91-13-840	3	
		Q17	. . Transistor, Germanium PNP	06228	2N1309	91-13-090	1	
		Q19, Q20, Q22	. . Transistor spec. no. 43223	00116		94-43-223	3	
		R1, R59	. . Resistor, fxd. comp. 390Ω 1/2W 5%	01121	EB3915	86-05-324	2	
		R2, R4	. . Resistor, fxd. comp. 10Ω 1/2W 5%	01121	EB1005	86-05-164	2	
		R3, R5	. . Resistor, fxd. comp. 2.7K 1/2W 5%	01121	EB2725	86-05-408	2	
		R6	. . Resistor, fxd. comp. 1K 2W 5%	01121	HB1025	86-07-364	1	
		R7	. . Resistor, fxd. comp. 10K 2W 5%	01121	HB1035	86-07-464	1	
		R8	. . Resistor, fxd. WW 15K 5W 5%	06136	5X1500	87-54-480	1	
		R9, R13, R49	. . Resistor, fxd. comp. 56K 1/4W 5%	01121	CB5635	86-04-540	3	
		R10, R14, R18	. . Resistor, fxd. comp. 27K 1/4W 5%	01121	CB2735	86-04-508	3	
		R11, R48	. . Resistor, fxd. comp. 6.8K 1/4W 5%	01121	CB6825	86-04-448	2	
		R12, R15, R23, R31, R42, R57, R64	. . Resistor, fxd. comp. 4.7K 1/4W 5%	01121	CB4725	86-04-432	7	
		R16	. . Resistor, fxd. comp. 8.2K 1/4W 5%	01121	CB8225	86-04-456	1	
		R17, R26, R36, R52	. . Resistor, fxd. comp. 15K 1/4W 5%	01121	CB1535	86-04-480	4	
		R19, R21, R27, R29, R38, R40	. . Resistor, fxd. comp. 30K 1/4W 5%	01121	CB3035	86-04-512	6	

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
		R20, R28, R39	. . Resistor, fxd. comp. 82K 1/4W 5%	01121	CB8235	86-04-556	3	
		R22, R30, R41, R50, R58	. . Resistor, fxd. comp. 100Ω 1/4W 5%	01121	CB1015	86-04-264	5	
		R24, R32, R34, R35, R43, R44	. . Resistor, fxd. comp. 1K 1/4W 5%	01121	CB1025	86-04-364	6	
		R25, R37, R53, R65, R67, R69, R72	. . Resistor, fxd. comp. 100K 1/4W 5%	01121	CB1045	86-04-564	7	
		R33, R45, R68	. . Resistor, fxd. comp. 24K 1/4W 5%	01121	CB2435	86-04-504	3	
		R46	. . Resistor, fxd. comp. 330Ω 1/4W 5%	01121	CB3315	86-04-316	1	
		R47	. . Res. fxd. comp. 2.2 meg. 1/4W 5%	01121	CB2255	86-04-696	1	
		R51, R55	. . Resistor, fxd. comp. 2.2K 1/4W 5%	01121	CB2225	86-04-396	2	
		R54	. . Resistor, fxd. comp. 120K 1/4W 5%	01121	CB1245	86-04-572	1	
		R56	. . Resistor, fxd. comp. 3.9K 1/4W 5%	01121	CB3925	86-04-424	1	
		R60	. . Resistor, fxd. comp. 12K 1/4W 5%	01121	CB1235	86-04-472	1	
		R61	. . Resistor, fxd. comp. 62K 1/2W 5%	01121	EB6235	86-05-544	1	
		R62	. . Resistor, fxd. comp. 100K 1/2W 5%	01121	EB1045	86-05-564	1	
		R63	. . Resistor, fxd. comp. 20K 1/4W 5%	01121	CB2035	86-04-492	1	
		R66	. . Resistor, fxd. comp. 18K 1/4W 5%	01121	CB1835	86-04-488	1	
		R70, R71	. . Resistor, fxd. comp. 68K 1/4W 5%	01121	CB6835	86-04-548	2	
		R73, R74	. . Resistor, fxd. comp. 75K 1/4W 5%	01121	CB7535	86-04-552	2	
		TP1	. . Test Point, brown	00779	3-582340-1	73-79-011	1	
		TP2	. . Test Point, red	00779	3-582340-2	73-79-012	1	
		TP3	. . Test Point, orange	00779	3-582340-3	73-79-013	1	
		TP4	. . Test Point, yellow	00779	3-582340-4	73-79-014	1	
		TP5	. . Test Point, green	00779	3-582340-5	73-79-015	1	
		TP6	. . Test Point, blue	00779	3-582340-6	73-79-016	1	
			Schematic (reference)			115-121		

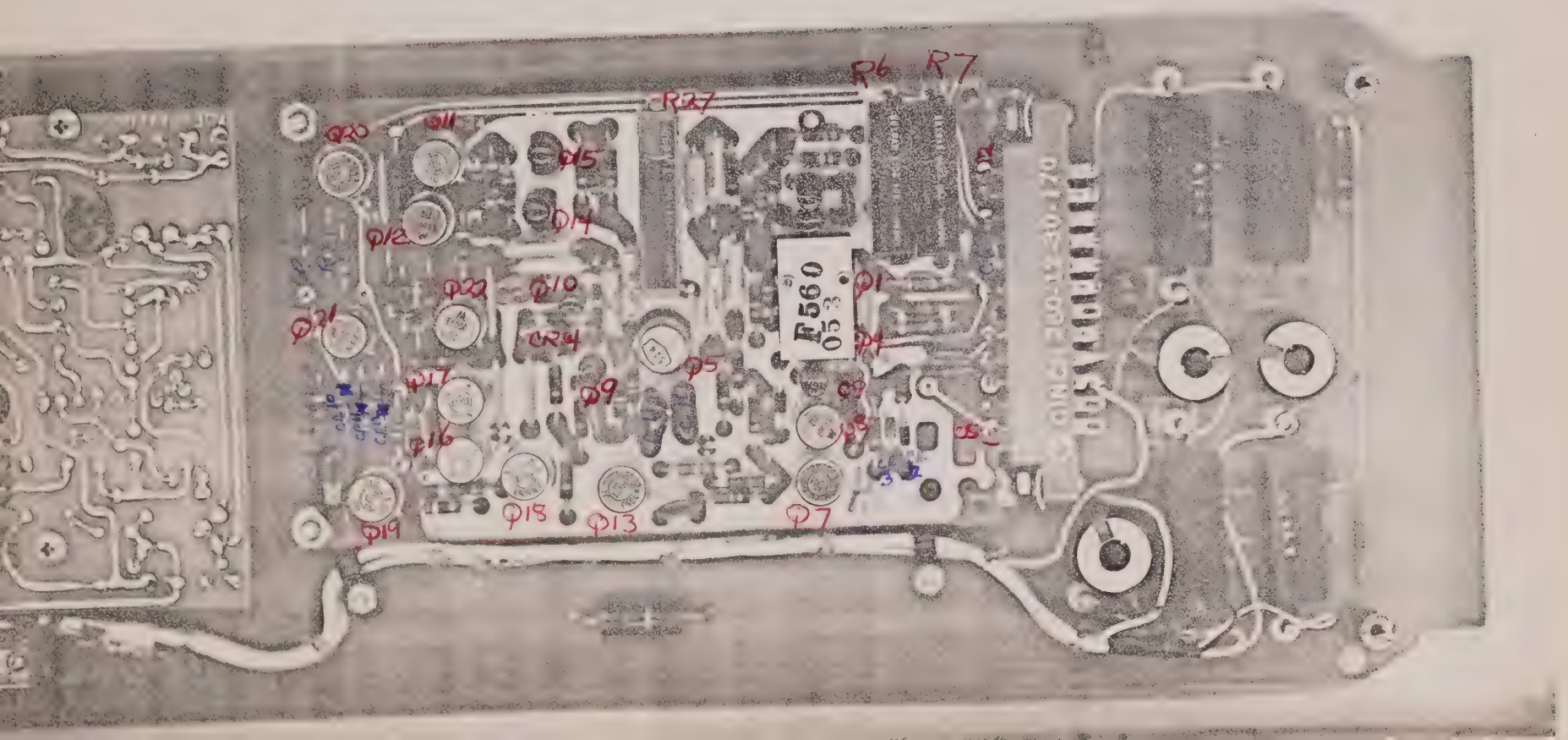
REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Decade and Symbol Driver Board Assy	00116		115-122-81	1	
			. . Handle	00116		00-35-024B	1	
		C101,C102,C201 C202,C301,C302 C401,C402,C501 C502,C701,C702 C801,C802,C901 C902, C1001, C1002, C1101, C1102	. . Capacitor, fxd. cer. 330μμF 50V	56289	40C207A	45-05-331	20	
		CR1 thru CR49, CR101, CR102, CR201, CR202, CR301, CR302, CR401, CR402, CR501, CR502, CR701, CR702, CR801, CR802, CR901, CR902, CR1001, CR1002, CR1101, CR1102	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	69	
		Q1 thru Q23	. . Transistor, spec. no. 43223	00116		91-43-223	23	
		Q101,Q102,Q201 Q202,Q301,Q302 Q401,Q402,Q501 Q502,Q701,Q702 Q801,Q802,Q901 Q902, Q1001, Q1002, Q1101, Q1102	. . Transistor, Germanium NPN	06228	2N1304	91-13-040	20	
		R1 thru R21	. . Resistor, fxd. comp. 100K 1/4W 5%	01121	CB1045	86-04-564	21	
		R22 thru R40	. . Resistor, fxd. comp. 20K 1/4W 5%	01121	CB2035	86-04-492	19	
		R101,R102,R201 R202,R301,R302 R401,R402,R501 R502,R701,R702 R801,R802,R901 R902, R1001, R1002, R1101, R1102	. . Resistor, fxd. comp. 4.7K 1/4W 5%	01121	CB4725	86-04-432	20	
		R103,R104,R203 R204,R303,R304 R403,R404,R503 R504,R703,R704 R803,R804,R903 R904, R1003, R1004, R1103, R1104	. . Resistor, fxd. comp. 24K 1/4W 5%	01121	CB2435	86-04-504	20	
		R105,R106,R205 R206,R305,R306 R405,R406,R505 R506,R705,R706 R805,R806,R905 R906, R1005, R1006, R1105, R1106	. . Resistor, fxd. comp. 62K 1/4W 5%	01121	CB6235	86-04-544	20	
			Schematic (reference)	00116		115-122		

REFERENCES FIG	REFERENCES IND	REFERENCES SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. *Decade & Nixie Driver Board Assy	00116		115-123-81	1	
			. . Handle	00116		00-36-024B	1	
		C101,C102,C201 C202,C301,C302 C401, C402	. . Capacitor, fxd. cer. 330μμF 50V	56289	40C207A	45-05-331	16	
		CR1 thru CR12, CR101, CR102, CR201, CR202, CR301, CR302, CR401, CR402,	. . Semicon. Device, Diode spec. no. 001 581-00	00116		94-45-581	42	
		Q1 thru Q12	. . Transistor spec. no. 43223	00116		91-43-223	24	
		Q101,Q102,Q201 Q202,Q301,Q302 Q401, Q402	. . Transistor, Germanium NPN	06228	2N1304	91-13-040	16	
		R1 thru R10	. . Resistor, fxd. comp. 100K 1/4W 5%	01121	CB1045	86-04-564	20	
		R11 thru R17	. . Resistor, fxd. comp. 20K 1/4W 5%	01121	CB2035	86-04-492	14	
		R101,R103,R201 R203,R301,R303 R401, R403	. . Resistor, fxd. comp. 4. 7K 1/4W 5%	01121	CB4725	86-04-432	16	
		R102,R104,R202 R204,R302,R304 R402, R404	. . Resistor, fxd. comp. 24K 1/4W 5%	01121	CB2435	86-04-504	16	
		R105,R106,R205 R206,R305,R306 R405, R406	. . Resistor, fxd. comp. 62K 1/4W 5%	01121	CB6235	86-04-544	16	
			*NOTE: Two Assemblies required per instrument.					
			Schematic (reference)	00116		115-123		

EI-85

GPA 1

GEN. PURPOSE AMP.



REFERENCES FIG	REFERENCES IND	REFERENCES SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Guard Crossing Assy	00116		115-120-81	1	
			. . Rail, Sliding side	00116		105-333-35	1	
			. . Shield, inside guard	00116		105-150-33	1	
			. . Shield, outside guard	00116		105-144-43	1	
			. . Support Bar	00116		115-442-31	4	
		C1, C4 thru C15	. . Capacitor, fxd. metmy. .047µF 200V	12406	ZX2A-473K	55-00-473	13	
		C2, C3	. . Capacitor, fxd. metallized paper .25 µF 100V	12406	VX1A-254	56-00-254	2	
		L1 thru L44 L49 thru L92	. . Inductor spec. no. 011-049-00	00116		96-43-700	88	
			. Outside Guard Crossing Assy	00116		115-125-82	1	
			. . Handle	00116		00-36-024B	1	
		CR1 thru CR15	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	15	
		R1 thru R29	. . Resistor, fxd. comp. 1K 1/4W 5%	01121	CB1025	86-04-364	29	
		R30 thru R43	. . Resistor, fxd. comp. 30K 1/4W 5%	01121	CB3035	86-04-512	15	
			. Inside Guard Crossing Assy	00116		115-126-81	1	
			. . Handle	00116		00-36-024B	1	
		C20 thru C48	. . Capacitor, fxd. cer. .0015µF 50V	56289	19C264	45-05-152	29	
		C49	. . Capacitor, fxd. ta. 50µF 20V	09213	Type 62F	63-02-506	1	
		CR20 thru CR48	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	29	
		R49 thru R64, R69, R71 thru R75	. . Resistor, fxd. comp. 510K 1/4W 5%	01121	CB5145	86-04-636	22	
		R65 thru R68, R70, R76, R77	. . Resistor, fxd. comp. 30K 1/4W 5%	01121	CB3035	86-04-512	7	
		R78, R79	. . Resistor, fxd. comp. 15K 1/4W 5%	01121	CB1535	86-04-480	2	
		R80 thru R94	. . Resistor, fxd. comp. 470Ω 1/4W 5%	01121	CB4715	86-04-332	15	
			Schematic (reference)	00116		115-120		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Inside Power Supply Board Assy	00116		115-127-83	1	
			. . Handle	00116		00-36-024B	1	
		C4 thru C10	. . Capacitor, fxd. elect. 50μF 50V	56289	30D200A1	61-05-506	7	
		C11	. . Capacitor, fxd. metmy. .47μF 200V	12406	ZX2A-474K	55-00-474	1	
		C12	. . Capacitor, fxd. elect. 100μF 12V	56289	30D154A1	61-02-107	1	
		C13	. . Capacitor, fxd. metmy. .047μF 200V	12406	ZX2A-473K	55-00-473	1	
		C14	. . Capacitor, fxd. elect. 50μF 25V	56289	30D186A1	61-04-506	1	
		C15	. . Capacitor, fxd. elect. 100μF 25V	56289	30D188A1	61-04-107	1	
		C16	. . Capacitor, fxd. cer. 220μμF 1000V	71590	DD-221	48-10-221	1	
		CR14 thru CR20, CR22 thru CR61, CR63 thru CR65	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	50	
		CR62	. . Semicon. Device, Diode	07910	1N753A	92-07-531	1	
		Q4 thru Q11	. . Transistor, Germanium PNP	09213	2N404A	91-04-043	8	
		Q12	. . Transistor, Germanium NPN	06228	2N1304	91-13-040	1	
		Q13, Q14, Q18	. . Transistor, Germanium PNP	49671	2N1183A	91-11-833	3	
		Q15, Q16	. . Transistor, Si. NPN	09213	2N3391	91-33-910	2	
		Q17	. . Transistor, Germanium PNP	06228	2N2188	91-21-880	1	
		R4, R7, R16, R17, R24, R25, R28, R29, R40, R62, R63, R64	. . Resistor, fxd. comp. 30K 1/4W 5%	01121	CB3035	86-04-512	12	
		R5, R8, R11, R14, R19, R22, R30, R36	. . Resistor, fxd. comp. 33K 1/4W 5%	01121	CB3335	86-04-516	8	
		R6, R9, R10, R15, R20, R23, R26, R31, R37	. . Resistor, fxd. comp. 150K 1/4W 5%	01121	CB1545	86-04-580	9	
		R12, R13, R18, R21	. . Resistor, fxd. comp. 12K 1/2W 5%	01121	EB1235	86-05-472	4	
		R27	. . Resistor, fxd. comp. 27K 1/4W 5%	01121	CB2735	86-04-508	1	
		R33, R38	. . Resistor, fxd. comp. 75K 1/4W 5%	01121	CB7535	86-04-552	2	
		R41	. . Resistor, fxd. comp. 10Ω 1W 5%	01121	GB1005	86-06-164	1	
		R42, R48	. . Resistor, fxd. comp. 15K 1/2W 5%	01121	EB1535	86-05-480	2	
		R43	. . Resistor, fxd. WW 1.5Ω 5W 5%	06136	5XM1.5	87-54-100	1	
		R44 thru R47	. . Resistor, fxd. comp. 9.1K 1/2W 5%	01121	EB9125	86-05-460	4	
		R49, R51	. . Resistor, fxd. comp. 1K 1/2W 5%	01121	EB1025	86-05-364	2	
		R52	. . Resistor, fxd. comp. 300Ω 1/2W 5%	01121	EB3015	86-05-312	1	
		R53	. . Resistor, fxd. comp. 47K 1/2W 5%	01121	EB4735	86-05-532	1	
		R55	. . Resistor, fxd. comp. 820Ω 1/2W 5%	01121	EB8215	86-05-356	1	
		R56	. . Resistor, fxd. comp. 33K 1/2W 5%	01121	EB3335	86-05-516	1	
		R57	. . Resistor, fxd. comp. 5.6K 1/2W 5%	01121	EB5625	86-05-440	1	
		R58, R60	. . Resistor, fxd. comp. 2.7K 1/2W 5%	01121	EB2725	86-05-412	2	
		R59	. . Resistor, fxd. comp. 3K 1/2W 5%	01121	EB3025	86-05-412	1	
		R61	. . Resistor, fxd. comp. 3.9K 1/2W 5%	01121	EB3925	86-05-424	1	

REFERENCES			DESCRIPTION	MANUFACTURER'S		HONEYWELL	QTY/	EFF.
FIG	IND	SCHEMATIC	1 2 3 4 5 6 7	CODE	PART NO.	PART NO.	ASSY	CODE
			. Inside Power Supply Board Assy(cont)					
		TP1	. . Test Point, brown	00779	3-582340-1	73-79-011	1	
		TP2	. . Test Point, red	00779	3-582340-2	73-79-012	1	
		TP3	. . Test Point, orange	00779	3-582340-3	73-79-013	1	
		TP4	. . Test Point, yellow	00779	3-582340-4	73-79-014	1	
		TP5	. . Test Point, green	00779	3-582340-5	73-79-015	1	
			Schematic (reference)	00116		115-127		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Sequencer 5 Digit Board Assy	00116		115-128-82	1	
			. . Handle	00116		00-36-024B	1	
		CR1 thru CR47, CR49 thru CR103, CR201 thru CR212, CR301 thru CR312, CR401 thru CR412, CR501 thru CR512, CR601 thru CR612, CR701 thru CR712, CR801 thru CR812, CR901 thru CR912, CR1001 thru CR1012	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	237	
		Q201, Q202, Q301, Q302, Q401, Q402, Q501, Q502, Q601, Q602, Q701, Q702, Q801, Q802, Q901, Q902, Q1001, Q1002	. . Transistor, Germanium PNP	09213	2N404A	91-04-043	18	
		R1, R3, R4, R6, R13, R14, R17, R18, R19, R21, R22, R23, R25, R26, R27, R29, R31, R32, R33, R34	. . Resistor, fxd. comp. 30K 1/4W 5%	01121	CB3035	86-04-512	20	
		R2, R7 thru R12, R15, R16, R20, R24, R28, R30, R35, R36, R201, R205, R301, R305, R401, R405, R501, R505, R601, R605, R701, R705, R801, R805, R901, R905, R1001, R1005	. . Resistor, fxd. comp. 150K 1/4W 5%	01121	CB1545	86-04-580	33	
		R5	. . Resistor, fxd. comp. 15K 1/4W 5%	01121	CB1535	86-04-480	1	
		R202 thru R204, R206 thru R208, R302 thru R304, R306 thru R308, R402 thru R404, R406 thru R408, R502 thru R504, R506 thru R508, R602 thru R604, R606 thru R608, R702 thru R704, R706 thru R708, R802 thru R804, R806 thru R808, R902 thru R904, R906 thru R908, R1002 thru R1004, R1006 thru R1008	. . Resistor, fxd. comp. 33K 1/4W 5%	01121	CB3335	86-04-516	54	
			Schematic (reference)	00116		115-128		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. 10^4, 10^3 Decade Board Assy	00116		115-129-81	1	
			. . Handle	00116		00-36-024B	1	
		CR1 thru CR22, CR24 thru CR35, CR39 thru CR51, CR54 thru CR97, CR99 thru CR100, CR102 thru CR134	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	127	
		Q1 thru Q12, Q14 thru Q21	. . Transistor, Germanium PNP	09213	2N404A	91-04-043	20	
		Q13	. . Transistor spec. no. 43223	00116		91-43-223	1	
		R1, R4, R10, R13, R19, R22, R31, R36, R39, R47, R51, R54, R59, R62, R68, R71, R75, R78, R83, R85	. . Resistor, fxd. comp. 27K 1/2W 5%	01121	EB2735	86-05-508	20	
		R2, R5, R11, R14, R20, R24, R29, R33, R37, R40, R52, R55, R60, R64, R69, R72, R76, R79	. . Resistor, fxd. comp. 33K 1/4W 5%	01121	CB3335	86-04-516	18	
		R3, R6, R12, R15, R21, R25, R30, R34, R38, R41, R48, R53, R56, R61, R65, R70, R73, R77, R80	. . Resistor, fxd. comp. 150K 1/4W 5%	01121	CB1545	86-04-580	19	
		R7, R8, R9, R17, R18, R26, R27, R35, R42, R43, R44, R45, R50, R57, R58, R66, R67, R74, R81, R82	. . Resistor, fxd. comp. 30K 1/4W 5%	01121	CB3035	86-04-512	20	
		R28	. . Resistor, fxd. comp. 15K 1/2W 5%	01121	EB1535	86-05-480	1	
		R46	. . Resistor, fxd. comp. 56K 1/4W 5%	01121	CB5635	86-04-540	1	
		R49	. . Resistor, fxd. comp. 15K 1/4W 5%	01121	CB1535	86-04-480	1	
		R84	. . Resistor, fxd. comp. 68K 1/4W 5%	01121	CB6835	86-04-548	1	
			Schematic (reference)	00116		115-129		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. 10^2, 10^1, 10^0 Decade Board Assy	00116		115-130-81	1	
			. . Handle	00116		00-36-024B	1	
		CR1 thru CR135	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	135	
		Q1 thru Q24	. . Transistor, Germanium PNP	09213	2N404A	91-04-043	24	
		R1, R4, R9, R12, R17, R20, R24, R27, R31, R34, R39, R42, R47, R50, R54, R57, R61, R64, R69, R72, R77, R80, R84, R87	. . Resistor, fxd. comp. 27K 1/2W 5%	01121	EB2735	86-05-508	24	
		R2, R4, R10, R13, R18, R21, R25, R28, R32, R35, R40, R43, R48, R51, R55, R58, R62, R65, R70, R73, R78, R81, R85, R88	. . Resistor, fxd. comp. 33K 1/4W 5%	01121	CB3335	86-04-516	24	
		R3, R6, R11, R14, R19, R22, R26, R29, R33, R36, R41, R44, R49, R52, R56, R59, R63, R66, R71, R74, R79, R82, R86, R89	. . Resistor, fxd. comp. 150K 1/4W 5%	01121	CB1545	86-04-580	24	
		R7, R8, R15, R16, R23, R30, R37, R38, R45, R46, R53, R60, R67, R68, R75, R76, R83, R90	. . Resistor, fxd. comp. 30K 1/4W 5%	01121	CB3035	86-04-512	18	
			Schematic (reference)	00116		115-130		

REFERENCES FIG	REFERENCES IND	REFERENCES SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Clock Board Assy	00116		115-131-82	1	
			. . Handle	00116		00-36-024B	1	
		C1	. . Capacitor,fxd.durmica . 005μF 500V	04062	DM-19-502J	53-09-502	1	
		C2	. . Capacitor,fxd.metmy . 047μF 200V	12406	ZX2A-473K	55-00-473	1	
		C3, C6, C13, C16, C17, C20	. . Capacitor,fxd.cer. 270μμF 1000V	71590	DD-270	48-10-271	6	
		C4, C5	. . Capacitor,fxd.cer. 330μμF 1000V	71590	DD-331	48-10-331	2	
		C7, C8, C9, C10, C12	. . Capacitor,fxd.cer. 220μμF 1000V	71590	DD-221	48-10-221	6	
		C14, C15, C18, C19	. . Capacitor,fxd.cer. 47μμF 1000V	71590	DD-471	48-10-471	4	
		CR1 thru CR113	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	113	
		Q1 thru Q24	. . Transistor, Germanium PNP	09213	2N404A	91-04-043	24	
		Q25	. . Transistor	14936	2N445A	91-04-453	1	
		R1, R4, R5, R7, R10, R13, R63, R66	. . Resistor, fxd. comp. 15K 1/2W 5%	01121	EB1535	86-05-480	8	
		R2, R8, R16, R21, R25, R29, R33, R37, R41, R45, R49, R52, R55, R58, R61, R64, R67, R71, R74, R80, R83, R90, R93	. . Resistor, fxd. comp. 33K 1/4W 5%	01121	CB3335	86-04-516	23	
		R3, R6	. . Resistor, fxd. comp. 22K 1/4W 5%	01121	CB2235	86-04-496	2	
		R9, R77, R86	. . Resistor, fxd. comp. 100K 1/4W 5%	01121	CB1045	86-04-564	3	
		R11, R14, R20, R23, R28, R31, R36, R39, R44, R47, R51, R54, R57, R60, R70, R73, R79, R82, R89, R92	. . Resistor, fxd. comp. 27K 1/4W 5%	01121	CB2735	86-04-508	20	
		R12, R15, R22, R26, R30, R34, R38, R42, R46, R50, R53, R56, R59, R62, R65, R68, R72, R75, R81, R84, R91, R94	. . Resistor, fxd. comp. 150K 1/4W 5%	01121	CB1545	86-04-580	22	
		R17, R18, R19, R24, R27, R32, R35, R40, R43, R48, R76, R85, R87, R88, R95, R96, R97, R98, R101, R102	. . Resistor, fxd. comp. 30K 1/4W 5%	01121	CB3035	86-04-512	20	
		R69, R78	. . Resistor, fxd. comp. 15K 1/4W 5%	01121	CB1535	86-04-580	2	
		R99	. . Resistor, fxd. comp. 56K 1/4W 5%	01121	CB5635	86-04-540	1	
		R100	. . Resistor, fxd. comp. 9. 1K 1/4W 5%	01121	CB9125	86-04-560	1	

REFERENCES			DESCRIPTION	MANUFACTURER'S		HONEYWELL	QTY/	EFF.
FIG	IND	SCHEMATIC	1 2 3 4 5 6 7	CODE	PART NO.	PART NO.	ASSY	CODE
		TP1	. . Test Point, brown	00779	3-582340-1	73-79-011	1	
		TP2	. . Test Point, red	00779	3-582340-2	73-79-012	1	
		TP3	. . Test Point, orange	00779	3-582340-3	73-79-013	1	
		TP4	. . Test Point, yellow	00779	3-582340-4	73-79-014	1	
		TP5	. . Test Point, green	00779	3-582340-5	73-79-015	1	
			Schematic (reference)	00116		115-131		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Program Logic Board Assy	00116		115-132-83	1	
			. . Handle	00116		00-36-024B	1	
		C1	. . Capacitor, fxd. ta. 25μF 50V	37942	Type TAP	64-61-256	1	
		C2	. . Capacitor, fxd. cer. .01μF 50V	56289	19C214A6	45-05-112	1	
		C3, C6	. . Capacitor, fxd. cer. 470μμF 1000V	71590	DD-473	48-10-473	2	
		C4	. . Capacitor, fxd. metmy . 5μF 200V	12406	ZX2A-504K	55-00-504	1	
		C5, C7	. . Capacitor, fxd. elect. 5μF 50V	56289	30D193A1	61-05-056	2	
		C8	. . Capacitor, fxd. metmy . 1μF 200V	12406	ZX2A-104K	55-00-104	1	
		C9	. . Capacitor, fxd. cer. .001μF 1000V	71590	DD-102	48-10-102	1	
		C10	. . Capacitor, fxd. cer. 270μμF 1000V	71590	DD-271	48-10-271	1	
		CR1 thru CR74, CR76, CR78 thru CR104	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	102	
		K27	. . Relay, 12V 960 ohm lamp Coil Nom.	A1000	342-1A	82-77-100	1	
		Q1, Q2	. . Transistor, Germanium PNP	49671	2N1384	91-13-840	2	
		Q3 thru Q7, Q9 thru Q22	. . Transistor, Germanium PNP	09213	2N404A	91-04-043	19	
		Q8	. . Transistor spec. no. 43223	00116		91-43-223	1	
		R1, R5, R6, R9, R14, R15, R18, R49, R68, R70, R74, R77, R83	. . Resistor, fxd. comp. 27K 1/4W 5%	01121	CB2735	86-04-508	13	
		R2	. . Resistor, fxd. comp. 10K 1/4W 5%	01121	CB1035	86-04-464	1	
		R3, R31	. . Resistor, fxd. comp. 56K 1/4W 5%	01121	CB5635	86-04-540	2	
		R4	. . Resistor, fxd. comp. 130K 1/4W 5%	01121	CB1345	86-04-576	1	
		R7, R10, R16, R19, R38, R52, R61, R63, R66, R71, R75, R78, R81	. . Resistor, fxd. comp. 33K 1/4W 5%	01121	CB3335	86-04-516	14	
		R8, R11, R13, R17, R20, R32, R39, R50, R53, R59, R64, R69, R72, R76, R79, R82 R84	. . Resistor, fxd. comp. 150K 1/4W 5%	01121	CB1545	86-04-580	17	
		R12, R48	. . Resistor, fxd. comp. 120K 1/4W 5%	01121	CB1245	86-04-572	2	
		R21, R35, R47, R55	. . Resistor, fxd. comp. 100K 1/4W 5%	01121	CB1045	86-04-564	4	
		R23 thru R30, R33, R34, R36, R62, R73, R80	. . Resistor, fxd. comp. 30K 1/4W 5%	01121	CB3035	86-04-512	14	
		R37, R40, R51, R54	. . Resistor, fxd. comp. 15K 1/4W 5%	01121	CB1535	86-04-480	4	
		R41	. . Resistor, fxd. comp. 100Ω 1/4W 5%	01121	CB1015	86-04-264	1	
		R42	. . Resistor, fxd. comp. 22K 1/4W 5%	01121	CB2235	86-04-496	1	
		R44	. . Resistor, fxd. comp. 7.5K 1/4W 5%	01121	CB7525	86-04-452	1	
		R45	. . Resistor, fxd. comp. 300K 1/4W 5%	01121	CB3045	86-04-612	1	
		R46	. . Resistor, fxd. comp. 91K 1/4W 5%	01121	CB9135	86-04-560	1	
		R57, R60	. . Resistor, fxd. comp. 11K 1/2W 5%	01121	EB1135	86-04-468	2	

REFERENCES			DESCRIPTION	MANUFACTURER'S		HONEYWELL	QTY/	EFF.
FIG	IND	SCHEMATIC	1 2 3 4 5 6 7	CODE	PART NO.	PART NO.	ASSY	CODE
			. Program Logic Board Assy (cont)					
		R65	. . Resistor, fxd. comp. 82K 1/4W 5%	01121	CB8235	86-04-556	1	
		R67	. . Resistor, fxd. comp. 5.6K 1/4W 5%	01121	CB5625	86-04-440	1	
		TP1	. . Test Point, brown	00779	3-582340-1	73-79-011	1	
		TP2	. . Test Point, red	00779	3-582340-2	73-79-012	1	
		TP3	. . Test Point, orange	00779	3-582340-3	73-79-013	1	
			Schematic (reference)	00116		115-132		

REFERENCES			DESCRIPTION	MANUFACTURER'S		HONEYWELL	QTY/	EFF.
FIG	IND	SCHEMATIC	1 2 3 4 5 6 7	CODE	PART NO.	PART NO.	ASSY	CODE
			. Range Logic Board Assy	00116		115-133-83	1	
			. . Handle	00116		00-36-024B	1	
		C1, C2, C3	. . Capacitor, fxd. cer. 1500μμF 1000V	71590	DD-152	48-10-152	3	
		C4 thru C9, C11 thru C17, C20, C24, C26, C30, C31, C32	. . Capacitor, fxd. cer. 220μμF 1000V	71590	DD-221	48-10-221	19	
		C10	. . Capacitor, fxd. cer. 560μμF 1000V	71590	DD-561	48-10-561	1	
		C18, C19, C21, C23, C27, C28	. . Capacitor, fxd. cer. .001μF 1000V	71590	DD-102	48-10-102	6	
		C22, C25, C27, C29, C33	. . Capacitor, fxd. cer. 470μμF 1000V	71590	DD-473	48-10-473	5	
		CR1 thru CR226	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	226	
		Q1 thru Q4, Q12, Q14 thru Q17, Q19, Q21 thru Q29	. . Transistor, Germanium PNP	09213	2N404A	91-04-043	19	
		Q5 thru Q11, Q13, Q18	. . Transistor, Germanium PNP	06228	2N2001	91-20-010	9	
		Q20	. . Transistor spec. no. 43223	00116		91-43-223	1	
		R1, R5, R9, R13, R17, R46, R49, R76, R77	. . Resistor, fxd. comp. 18K 1/4W 5%	01121	CB1835	86-04-488	9	
		R2, R6, R10, R14, R18, R25, R50, R78, R83, R106, R107, R108, R109, R115	. . Resistor, fxd. comp. 15K 1/4W 5%	01121	CB1535	86-04-480	14	
		R3, R7, R11, R15, R19, R23, R27, R53 thru R64, R121, R130, R133, R134, R143, R144, R147, R148	. . Resistor, fxd. comp. 100K 1/4W 5%	01121	CB1045	86-04-564	27	
		R4, R8, R12, R16, R20, R24, R28, R32, R36, R40, R44, R48, R52, R94, R104	. . Resistor, fxd. comp. 56K 1/4W 5%	01121	CB5635	86-04-540	15	
		R21	. . Resistor, fxd. comp. 12K 1/2W 5%	01121	EB1235	86-05-472	1	
		R22	. . Resistor, fxd. comp. 10K 1/4W 5%	01121	CB1035	86-04-464	1	
		R26	. . Resistor, fxd. comp. 12K 1/4W 5%	01121	CB1235	86-04-472	1	
		R29, R37, R41, R96, R97, R100, R115	. . Resistor, fxd. comp. 33K 1/4W 5%	01121	CB3335	86-04-516	7	
		R30, R34, R38, R42, R71, R74, R101, R110, R112, R113, R114, R116, R119, R120, R124, R127, R131, R132, R137, R140, R145, R146, R151, R154,	. . Resistor, fxd. comp. 30K 1/4W 5%	01121	CB3035	86-04-512	24	

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Range Logic Board Assy (cont)					
		R31, R35, R39, R43, R47, R51, R66, R72, R75, R79, R84, R89, R98, R102, R117, R125, R129, R138, R141, R152, R155	. . Resistor, fxd. comp. 150K 1/4W 5%	01121	CB1545	86-04-580	21	
		R33, R123, R136	. . Resistor, fxd. comp. 15K 1/2W 5%	01121	EB1535	86-05-480	3	
		R45, R68, R88	. . Resistor, fxd. comp. 20K 1/4W 5%	01121	CB2035	86-04-492	3	
		R65, R105	. . Resistor, fxd. comp. 120K 1/4W 5%	01121	CB1245	86-04-572	2	
		R67, R70, R73, R80, R85, R90, R95, R99, R103, R118, R126, R139, R150, R153	. . Resistor, fxd. comp. 27K 1/4W 5%	01121	CB2735	86-04-508	14	
		R69	. . Resistor, fxd. comp. 36K 1/4W 5%	01121	CB3635	86-04-520	1	
		R81, R82	. . Resistor, fxd. comp. 16K 1/4W 5%	01121	CB1635	86-04-482	2	
		R86, R87	. . Resistor, fxd. comp. 22K 1/4W 5%	01121	CB2235	86-04-496	2	
		R91, R92, R93	. . Resistor, fxd. comp. 39K 1/4W 5%	01121	CB3935	86-04-524	3	
		R122, R128, R135, R142, R149	. . Resistor, fxd. comp. 470K 1/4W 5%	01121	CB4745	86-04-632	5	
			Schematic (reference)	00116		115-133		

REFERENCES FIG	REFERENCES IND	REFERENCES SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Bridge Board Assy	00116		115-134-81	1	
			. . Handle	00116		00-36-024B	1	
		CR1 thru CR42	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	42	
		Q1 thru Q42	. . Transistor	87216	2N2374	91-23-740	42	
		R1, R4, R7, R10, R13, R16, R18	. . Resistor, fxd. WW matched set (4) 200K, (1) 400K, (1) 800K, (1) 360K 1/2W .01% spec. no. 012-269-99	00116		12-26-999	1	
		R2	. . Resistor, fxd. comp. 10Ω 1/4W 5%	00116	CB1005	86-04-164	1	
		R5, R6, R8, R9, R11, R12, R14, R15, R17, R19, R21, R22, R24, R25, R27, R28, R30, R32	. . Resistor, fxd. comp. 75K 1/4W 5%	01121	CB7535	86-04-552	18	
		R20, R26, R33, R37, R44, R50, R57, R63	. . Resistor, fxd. WW 200K 1/2W .01%	00116		12-26-430	8	
		R23, R34, R47, R60	. . Resistor, fxd. WW 100K 1/2W .01%	00116		12-26-270	4	
		R29, R40, R53, R66, R68	. . Resistor, fxd. WW 400K 1/2W .01%	00116		12-26-530	5	
		R31, R42, R55	. . Resistor, fxd. WW 360K 1/2W .01%	00116		12-26-510	3	
		R34, R35, R36, R38, R39, R41, R43, R45, R46, R48, R49, R51, R52, R54, R56, R58, R59, R61, R62, R64, R65, R67, R70, R73	. . Resistor, fxd. comp. 330K 1/4W 5%	01121	CB3345	86-04-616	24	
		R71	. . Resistor, fxd. comp. 5.1K 1/4W 5%	01121	CB5125	86-04-436	1	
		R72	. . Resistor, fxd. comp. 39K 1/4W 5%	01121	CB3935	86-04-524	1	
		R72	. . Resistor, fxd. WW 1K 1/4W 1%	00116		12-11-460	1	
		TP1	. . Test Point, brown	00779	3-582340-1	73-79-011	1	
		TP2	. . Test Point, red	00779	3-582340-2	73-79-012	1	
			Schematic (reference)	00116		115-134		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Input Function & Range Switching Board Assy	00116		115-135-85	1	
			. . Angle Bracket	73734	129520	74-08-125	2	
			. . Handle	00116		00-36-024B	1	
			. . Connector, Coaxial	71785	235-09-00-101	70-20-208	1	
			(Mating Connector)	71785	236-09-00-101	70-20-210		
			. . Connector, Receptacle	A3000	R0-2M9	70-33-010	1	
			(Mating Connector)	A3000	P0-2M9	70-33-020		
			. . Shield	00116		115-433-30	1	
			. . Connector Mtg. Bar	00116		115-431-31	1	
			. . Connector Mtg. Bar	00116		115-432-32	1	
		C6, C7	. . Capacitor, fxd. elect. 10μF 15V	56289	30D165A1	61-03-106	2	
		CR36, CR37, CR40, CR42, CR44, CR53, CR54	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	8	
		CR45 thru CR48	. . Semicon. Device, Diode spec. no. 001-580-00	00116		94-45-580	4	
		CR49 thru CR52	. . Semicon. Device, Diode	73293	1N126	92-01-260	4	
		K1	. . Reed Relay	A2000	12001	82-73-000	1	
		K2, K4, K7, K8	. . Reed Relay spec. no. 011-024-00	00116		82-73-203	4	
			. . Coil spec. no. 082-732-04	00116		82-73-204	4	
		K3-K3A, K6-K6A	. . Relay	09026	BR16-190-B-11-12V	82-10-015	2	
		Q1	. . Transistor, Germanium	04713	2N652	91-06-520	1	
		R87	. . Resistor, fxd. metflm. 100K 1/4W 1%	75042	MEB T8 100K 1%	83-36-780	1	
		R88	. . Resistor, fxd. metflm. 900K 1/4W 1%	75042	MEB T8 900K 1%	83-36-980	1	
		R89, R91, R93	. . Resistor, fxd. WW SET. (4) 2.25 meg (1) 899K, (1) 99.9K 1/2W .05%	00116		12-25-811	1	
		R90	. . Resistor, Variable 2K 1/2W 10%	80294	200L-1-202	88-20-564	1	
		R92	. . Resistor, Variable 200Ω 1/2W 10%	80294	200L-1-201	88-20-350	1	
		R94, R95	. . Resistor, fxd. metflm. 200K 1/2W 1%	94271	2003F	83-44-838	2	
		R96, R97	. . Resistor, fxd. comp. 220Ω 1/4W 5%	01121	CB2225	86-04-296	2	
		R98, R140	. . Resistor, fxd. comp. 1K 1/4W 5%	01121	CB1025	86-04-364	2	
		R99	. . Resistor, fxd. comp. 910Ω 1/4W 5%	01121	CB9125	86-04-360	1	
			Schematic (reference)	00116		115-148		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Reference Supply & Buffer Amplifier Board Assy	00116		115-136-82	1	
			. . Angle Bracket	72653	6261	74-08-001	2	
			. . Handle	00116		00-36-024B	1	
			. . Connector, 12 pin	71785	250-12-30-170	70-20-221	1	
			. . Shield Can	00116		115-435-13	1	
		C15	. . Capacitor, fxd. durmica 200μμF 500V	04062	DM-10-201J	53-02-201	1	
		CR31 thru CR34	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	4	
		K15 thru K18	. . Reed Relay	A2000	12001	82-73-000	4	
		R73	. . Resistor, Variable 10K 1/2W 10% ("0" Absol.)	80294	3067P-1-103	88-20-836	1	
		R74	. . Resistor, fxd. comp. 5.1K 1/4W 5%	01121	CB5125	86-04-436	1	
		R75	. . Resistor, fxd. comp. 100Ω 1/4W 5%	01121	CB1015	86-04-264	1	
		R76, R78, R80	. . Resistor, fxd. WWSET (2) 100K					
			(1) 99.95K 1/2W .01%	00116		12-26-998	1	
		R77	. . Resistor, Variable 100Ω 1W 10% (Ratio Absol.)	80294	260S-1-101	88-20-296	1	
		R79	. . Resistor, Variable 50Ω 1W 10% (+DC Absol.)	80294	260S-1-500	88-20-219	1	
		R83, R84	. . Resistor, fxd. comp. 2K 1/2W 5%	01121	EB2025	86-05-392	2	
			. . Resistor, fxd. comp. 1.2K 1W 5%	01121	GB1225	86-06-372	1	
		TP1	. . Test Point, brown	00779	3-582340-1	73-79-011	1	
		TP2	. . Test Point, red	00779	3-582340-2	73-79-012	1	
			Schematic (reference)	00116		115-148		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. RS-10 Reference Supply Board Assy	00116		115-143-82	1	
		C1	. . Capacitor, fxd. cer. 560μμF 1000V	71590	DD-561	48-10-561	1	
		C2	. . Capacitor, fxd. cer. 220μμF 1000V	71590	DD-221	48-10-221	1	
		CR1	. . Semicon. Device, Diode	04713	1N821	92-08-210	1	
		CR2 thru CR6	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	5	
		CR7	. . Semicon. Device, Diode spec. no. 43273	00116		94-43-273	1	
		Q1, Q3, Q4	. . Transistor, Si. NPN	09213	2N3391	91-33-910	3	
		Q2	. . Transistor, Si. PNP	07263	2N3638	91-36-380	1	
		Q5	. . Transistor spec. no. 001-514-00	00116		94-60-240	1	
		R1	. . Resistor, fxd. comp. 1.8K 1/4W 5%	01121	CB1825	86-04-388	1	
		R2	. . Resistor, fxd. comp. 12 meg 1/2W 5%	01121	EB1275	86-05-772	1	
		R3	. . Res. fxd. comp. 150Ω 1/4W 5%	01121	CB1525	86-04-280	1	
		R4	. . Res. fxd. metflm. 22.1K 1/8W 1%	75042	MEA T9 22.1K 1%	83-07-555	1	
		R5	. . Res. fxd. comp. 1K 1/4W 5%	01121	CB1025	86-04-364	1	
		R6	. . Res. fxd. comp. 220K 1/4W 5%	01121	CB2245	86-04-596	1	
		R7	. . Resistor, fxd. comp. 220Ω 1/4W 5%	01121	CB2215	86-04-296	1	
		R8	. . Resistor, fxd. comp. 2.7K 1/4W 5%	01121	CB2725	86-04-408	1	
		R9	. . Res., fxd. metflm. 10K 1/8W 1%	75042	MEA T9 10K 1%	83-07-533	1	
		R10	. . Res. fxd. metflm. 2.37K 1/8W 1%	75042	MEA T9 2.37K 1%	83-07-490	1	
		R11, R17	. . Res. fxd. comp. 56Ω 1/4W 5%	01121	CB5615	86-04-240	2	
		R14	. . Res. fxd. metflm. 12.4K 1/8W 1%	75042	MEA T9 12.4K 1%	83-07-536	1	
		R15	. . Res. fxd. metflm. 6.49K 1/8W 1%	75042	MEA T9 6.49K 1%	83-07-530	1	
		R16	. . Res. Variable 100Ω 1/2W 10%	90294	3067P-1-101	88-20-306	1	
		R18	. . Res. fxd. metflm. 2.74K 1/8W 1%	75042	MEA T9 2.74K 1%	83-07-499	1	
		R21	. . Res. fxd. WW 500Ω 1/4W .5%	00116		12-12-280	1	
		R22	. . SOT	00116		299-000-14	1	
		R23	. . SOT	00116		299-000-15	1	
		R24	. . Res. fxd. WW 6.2K 1/4W .05%	00116		12-15-621	1	
		R25	. . Res. fxd. metflm. 1.27 meg 1/2W 1%	75042	MEB T9 1.27meg 1%	83-58-900	1	
		R26	. . Resistor, Variable 10K 1/2W 10%	80294	200P-1-103	88-20-770	1	
		R12, R13, R19, R20	. . SOT					
			Schematic (reference)	00116		115-143		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. GPA-1 Board Assy	00116		501-100-86	1	
			. . Heatsink	00116		501-300-30	1	
			. . Switch Spacer	71590	P325	95-05-525	2	
		C1, C9	. . Cap. fxd. glass 15μμF 300V	07115	TY-06-150J	51-19-150	2	
		C2, C6, C7	. . Cap. fxd. cer. .01μF 50V	56289	19C214A6	45-05-112	3	
		C4, C5	. . Cap. fxd. cer. .001μF 1000V	71590	DD-102	48-10-102	2	
		C8, C10, C11	. . Cap. fxd. durmica 330μμF 500V	04062	DM-15-331J	53-01-331	3	
		CR1 thru CR4,	. . Semicon. Device, Diode					
		CR7, CR13, CR14	spec. no. 001-581-00	00116		94-45-581	7	
		CR5, CR6, CR8	. . Semicon. Device, Diode	07910	1N754A	92-07-541	3	
		CR9 thru CR12	. . Semicon. Device, Diode	73293	1N456	92-04-560	4	
		Q1, Q2, Q3, Q6, Q9, Q10	. . Transistor, Si. NPN	09213	2N3391	91-33-910	6	
		Q4A, Q4B	. . Transistor spec. no. 001-530-00	00116		94-60-230	1	
		Q5Q, Q5B	. . Transistor spec. no. 001-540-00	00116		94-60-240	1	
		Q7, Q11, Q13, Q16, Q17, Q18, Q19, Q20	. . Transistor, Si. NPN	49671	40053	94-65-053	8	
		Q8, Q12, Q21, Q22	. . Transistor spec. no. 001-507-00	00116		94-58-507	4	
		Q14, Q15	. . Transistor, Si. PNP	07263	2N3640	91-36-400	2	
		R1, R11	. . Res. fxd. comp. 1 meg 1/4W 5%	01121	CB1055	86-04-664	2	
		R2, R29, R30	. . Res. fxd. comp. 100K 1/4W 5%	01121	CB1045	86-04-564	3	
		R3, R14, R15	. . Res. fxd. comp. 10 meg 1/4W 5%	01121	CB1065	86-04-764	3	
		R4, R5	. . Res. fxd. comp. 2.2K 1/4W 5%	01121	CB2225	86-04-396	2	
		R6, R7	. . Res. Variable 200K 1/5W 20%	80294	3068P-1-204	88-20-966	2	
		R8	. . Res. fxd. comp. 47K 1/4W 5%	01121	CB4735	86-04-532	1	
		R9, R10	. . Res. fxd. comp. 100 meg 1/4W 5%	01121	CB1075	86-04-864	2	
		R12, R13	. . Res. fxd. metflm. 499K 1/8W 1%	75042	MEA T9 499K 1%	83-07-900	2	
		R16, R17	. . Res. fxd. comp. 3K 1/4W 5%	01121	CB3025	86-04-412	2	
		R18, R48	. . Res. fxd. comp. 22K 1/4W 5%	01121	CB2235	86-04-496	2	
		R19	. . Res. fxd. comp. 3.3K 1/4W 5%	01121	CB3325	86-04-416	1	
		R20	. . Res. fxd. comp. 15K 1/4W 5%	01121	CB1535	86-04-480	1	
		R21, R22	. . Res. fxd. metflm. 100K 1/8W 1%	75042	MEA T9 100K 1%	83-07-780	2	
		R23, R24	. . Res. fxd. metflm. 1K 1/8W 1%	75042	MEA T9 1K 1%	83-07-386	2	
		R25	. . Res. fxd. metflm. 249K 1/8W 1%	75042	MEA T9 249K 1%	83-07-824	1	
		R26	. . SOT					
		R27	. . Res. Variable 10K 1/2W 10%	80294	200P-1-103	88-20-770	1	
		R31, R32	. . Res. fxd. comp. 1K 1/4W 5%	01121	CB1025	86-04-364	2	
		R33	. . Res. fxd. comp. 12K 1/4W 5%	01121	CB1235	86-04-472	1	
		R34, R35, R53	. . Res. fxd. comp. 10K 1/4W 5%	01121	CB1035	86-04-464	3	

REFERENCES FIG	REFERENCES IND	REFERENCES SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. GPA-1 Board Assy (cont)					
		R36	. . Res. fxd. comp. 820Ω 1/4W 5%	01121	CB8215	86-04-356	1	
		R37, R43, R47	. . Res. fxd. comp. 2K 1/4W 5%	01121	CB2025	86-04-392	3	
		R38, R50	. . Res. fxd. comp. 3.9K 1/4W 5%	01121	CB3925	86-04-424	2	
		R39, R45, R46	. . Res. fxd. comp. 1.8K 1/4W 5%	01121	CB1825	86-04-388	3	
		R40, R41	. . Res. fxd. comp. 4.7K 1/4W 5%	01121	CB4725	86-04-432	2	
		R42	. . Res. fxd. comp. 33K 1/4W 5%	01121	CB3335	86-04-516	1	
		R44	. . Res. fxd. comp. 150Ω 1/4W 5%	01121	CB1515	86-04-280	1	
		R49	. . Res. fxd. comp. 390Ω 1/4W 5%	01121	CB3915	86-04-324	1	
		R51	. . Res. fxd. comp. 22Ω 1/4W 5%	01121	CB2205	86-04-196	1	
		R52	. . Res. fxd. comp. 18Ω 1/4W 5%	01121	CB1805	86-04-188	1	
			Schematic (reference)	00116		501-100		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Null Detector Board Assy	00116		115-137-85	1	
			. . Diode Mtg. Block	00116		115-426-31	1	
			. . Shield Can	00116		115-435-33	1	
			. . Handle	00116		00-36-024B	1	
			. . Connector	71785	250-12-30-170	70-20-221	1	
			. . Angle Bracket	72653	6261	74-08-001	2	
		C8	. . Cap. fxd. poly. .209μF 200V	12406	PD2A-2093F	60-01-209	1	
		C9	. . Cap. fxd. poly. .036μF 100V	12406	PD1A-363F	60-01-036	1	
		C10	. . Cap. fxd. poly. .273μF 200V	12406	PD2A02733F	60-01-273	1	
		C11	. . Cap. fxd. durmica 1000μμF 500V	04062	DM-15-102J	53-01-102	1	
		C12	. . Cap. fxd. glass 100μμF	07115	CY-15-151K	51-96-101	1	
		C13	. . Cap. fxd. poly. .1μF 100V	12406	PD1A-104F	60-01-105	1	
		C16	. . Cap. fxd. cer. .001μF 1000V	71590	DD-102	48-10-102	1	
		C17	. . Cap. fxd. durmica 2μμF 500V	04062	DM-10-020	53-02-020	1	
		C18	. . Cap. fxd. cer. 10μμF 1000V	71590	DD-100	48-10-100	1	
		CR55, CR58, CR59, CR60, CR77, CR79, CR80	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	7	
		CR67 thru CR70	. . Semicon. Device, Diode	09213	1N916	92-09-160	4	
		CR71, CR72	. . Semicon. Device, Diode	73293	1N456	92-04-560	2	
		CR76, CR78	. . Semicon. Device, Diode	07910	1N754A	92-07-541	2	
		K9, K13	. . Relay 12V 960 ohm lamp Coil	A1000	342-1A	82-77-100	2	
		K9A	. . Relay, Reed	15636	R1516-2	82-73-002	1	
		K10, K11, K12	. . Reed, Switch, Glass spec. no. 011-029-00	00116		95-73-013	3	
		K14	. . Reed Switch, Glass spec. no. 011-028-00	00116		95-73-016	1	
		Q1-Q2	. . Transistor, Dual Differential spec. no. 001-513-00	00116		94-60-230	1	
		Q3, Q5, Q6, Q8, Q9	. . Transistor, Si. NPN	09213	2N3391	91-33-910	5	
		Q4, Q7	. . Transistor, Si. PNP	07263	2N3640	91-36-400	2	
		Q10, Q11	. . Transistor, Germanium PNP	09213	2N404A	91-04-043	2	
		R100, R143, R146 R148	. . Res. fxd. metflm. 100K 1/8W 1%	75042	MEA T9 100K 1%	83-07-780	4	
		R101	. . Res. fxd. comp. 100Ω 1/4W 5%	01121	CB1015	86-04-264	1	
		R102, R103	. . Res. fxd. comp. 2K 1/2W 5%	01121	EB2025	86-05-392	2	
		R105	. . Res. fxd. comp. 100K 1/4W 5%	01121	CB1045	86-05-564	1	
		R106, R110	. . Resistor, fxd. WW SET (1) 100. 4K (1) 900K 1/2W .01%	00116		12-26-962	1	
		R107	. . Res. fxd. comp. 22 meg 1/4W 5%	01121	CB2265	86-04-796	1	
		R108	. . Res. fxd. comp. 10Ω 1/4W 5%	01121	CB1005	86-04-164	1	
		R109	. . Res. Variable 100Ω 1/2W 10% (F.S. 1V)	80294	200P-1-101	88-20-285	1	

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Null Detector Board Assy (cont)					
		R111, R114, R115, R118	. . Res. fxd. comp. 200K 1/4W 5%	01121	CB2045	86-04-592	4	
		R119, R120	. . Res. fxd. comp. 27K 1/4W 5%	01121	CB2735	86-04-508	2	
		R121, R139, , R153, R164	. . Res. fxd. comp. 12K 1/4W 5%	01121	CB1235	86-04-472	5	
		R126, R144	. . Res. fxd. comp. 39 meg 1/4W 5%	01121	CB3965	86-04-725	2	
		R127, R129	. . Res. fxd. metflm. 1K 1/8W 1%	75042	MEA T9 1K 1%	83-07-386	2	
		R12 , R141	. . Res. fxd. comp. 2. 7K 1/4W 5%	01121	CB2725	86-04-408	2	
		R128, R132	. . Res. fxd. WW SET 20K 1/2W . 1% Matched Pair	00116		12-24-401	1	
		R130	. . Resistor, fxd. 10 meg 1/4W 5%	01121	CB1065	86-04-764	1	
		R131	. . Res. fxd. metflm. 806K 1/4W 1%	75042	MEB T9 806K 1%	83-38-960	1	
		R133	. . Res. fxd. metflm. 7. 68K 1/8W 1%	75042	MEA T9 7. 68K 1%	83-07-531	1	
		R134	. . Res. fxd. metflm. 2. 49K 1/8W 1%	75042	MEA T9 2. 49K 1%	83-07-495	1	
		R135, R137	. . Res. fxd. comp. 220K 1/4W 5%	01121	CB2245	86-04-596	2	
		R136	. . Res. Variable 5K 1/2W 10%(ZERO)	80294	200P-1-502	88-20-700	1	
		R138	. . Res. fxd. comp. 2K 1/4W 5%	01121	CB2025	86-04-392	1	
		R144	. . Res. fxd. metflm. 20K 1/8W 1%	75042	MEA T9 20K 1%	83-07-550	1	
		R145	. . Res. Variable 100K 1/5W 20% ("0" 1V Rng)	80294	3068P-1-104	88-20-951	1	
		R145, R158, R160	. . Res. fxd. metflm. 1K 1/8W 1%	75042	MEA T9 1K 1%	83-07-364	3	
		R147	. . Res. fxd. WW 1K 1/4W 1%	00116		12-11-460	1	
		R151, R155, R157 R168	. . Res. fxd. comp. 3. 3K 1/4W 5%	01121	CB3325	86-04-416	4	
		R152, R154	. . Res. fxd. comp. 3. 9K 1/4W 5%	01121	CB3925	86-04-424	2	
		R159, R161	. . Res. fxd. comp. 47Ω 1/4W 5%	01121	CB4715	86-04-232	2	
		R162, R163	. . Res. fxd. comp. 22K 1/4W 5%	01121	CB2235	86-04-496	2	
		R165, R167	. . Res. fxd. comp. 10K 1/4W 5%	01121	CB1035	86-04-464	2	
		R166	. . Res. fxd. comp. 3. 6K 1/4W 5%	01121	CB3625	86-04-420	1	
		TP1	. . Test Point, brown	00779	3-582340-1	73-79-011	1	
		R112, R113, R116, R117, R123, R124, R139, R140, R142, R147	. . SOT					
			Schematic (reference)	00116		115-137 & 115-148		

REFERENCES FIG	REFERENCES IND	REFERENCES SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			OPTIONAL OPERATIONAL FEATURES					
			Due to the wide variety of options available for the Model EI-85 all or part of the assemblies listed below may or may not be included in your instrument.					
			OPTIONS:					
			Model 85-00-13					
			Ohms Pre Amplifier Board Assy			115-138-83		
			Pre Amplifier Board Assembly			115-138-62		
			GPA-1 Board Assembly			501-100-86		
			Temp. Comp. Board Assembly			115-145-82		
			Ohms Attenuator Board Assembly			115-142-83		
			Model 85-00-1					
			Ohms Board Assembly			115-146-80		
			GPA-1 Board Assembly			501-100-86		
			Ohms Attenuator Board Assembly			115-142-83		
			Model 85-00-2					
			AC-1 Converter Board Assembly			115-144-83		
			Model 85-00-3					
			Pre Amplifier Board Assembly			115-138-62		
			GPA-1 Board Assembly			501-100-86		
			Temp-Comp. Board Assembly			115-145-82		
			OTHER AVAILABLE OPTIONS:					
			Decade and Nixie Driver 8421 Pos. True Board Assembly			115-153-80		
			Decade and Symbol Driver 8421 Pos. True Board Assembly			115-151-80		
			Negative True Print Command Outside Power Supply Board Assembly			115-158-80		
			Decade and Symbol Driver 8421 Negative True Board Assembly			115-152-80		
			Decade and Nixie Driver 8421 Negative True Board Assembly			115-154-80		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Ohms Pre Amplifier Board Assy	00116		115-138-83	1	
			. . Pre Amplifier Board Assy	00116		115-138-61	1	
			. . Ohms Attenuator Board Assy	00116		115-142-83	1	
			. Pre Amplifier Board Assy	00116		115-138-61	1	
			. . Handle	00116		00-24-036B	1	
			. . Connector Mtg. Bar	00116		115-412-30	1	
			. . Connector, Coaxial	71785	235-09-00-101	70-20-208	1	
			(Mating Connector)	71785	236-09-00-101	70-20-210		
			. . Pre Amplifier & Ohms Shield	00116		115-411-30	1	
			. . Connector	71785	250-12-30-170	70-20-221	1	
			. . Angle Bracket	72653	6261	74-08-001	2	
		C1	. . Cap. fxd. poly. .047μF 100V	12406	PD1A-473K	60-01-473	1	
		C2	. . Cap. fxd. durmica .001μF 500V	04062	DM-15-102J	53-01-102	1	
		CR1, CR76	. . Semicon. Device, Diode spec. no. 001-580-00	00116		94-45-580	2	
		CR2 thru CR5	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	4	
		K19-K19A, K19B-K19C	. . Relay	82768	TQ1011	82-04-750	1	
		K20	. . Relay	09026	BR-16-190-B-11-12-V	82-10-015	1	
		R1, R2	. . Res. fxd. comp. 100K 1/4W 5%	01121	CB1045	86-04-564	2	
		R3	. . Res. fxd. comp. 10K 1/2W 5%	01121	EB1035	86-05-464	1	
		R4, R9	. . Res. fxd. WW SET 1K, 98.85K, 1/2W .01%	00116		12-26-961	2	
		R5, R6, R7	. . Res. fxd. comp. 10K 1/4W 5%	01121	CB1035	86-04-464	3	
		R8	. . Res. Variable 100Ω 1/2W 10% (F.S. .1V Rng)	80294	3067P-1-101	88-20-306	1	
		R10	. . Res. fxd. comp. 10 meg 1/4W 5%	01121	CB1065	86-04-764	1	
		R11	. . Res. fxd. comp. 1 meg 1/4W 5%	01121	CB1055	86-04-664	1	
		R12	. . Res. fxd. comp. 150Ω 1/4W 5%	01121	CB1515	86-04-280	1	
		R13	. . Res. fxd. comp. 5.1K 1/4W 5%	01121	CB5125	86-04-436	1	
		R14	. . Res. Variable 10Ω 1W 10%	80294	260P-1-100	88-20-085	1	
		R81, R82	. . Res. fxd. comp. 2K 1/2W 5%	01121	EB2025	86-05-392	2	
		R145	. . Res. fxd. comp. 100Ω 1/4W 5%	01121	CB1015	86-04-263	1	
		R146	. . Res. fxd. comp. 200Ω 1/2W 5%	01121	EB2015	86-05-292	1	
			Schematic (reference)	00116		115-148		

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Temperature Compensation Board Assy	00116		115-145-82	1	
			. . Diode Mtg. Bracket	00116		115-426-31	1	
		CR6, CR7	. . Semicon. Device, Diode	07910	1N754A	92-07-541	2	
		CR73, CR74	. . Semicon. Device, Diode	73293	1N456	92-04-560	2	
		R16, R28	. . Res. fxd. comp. 7.5K 1/2W 5%	01121	EB7525	86-05-452	2	
		R17, R27	. . Res. fxd. comp. 27K 1/4W 5%	01121	CB2735	86-04-472	2	
		R20, R26	. . Res. fxd. metflm. 2.74K 1/8W 1%	75042	MEA T9 2.74K 1%	83-07-499	2	
		R21	. . Res. Variable 200K 1/5W 20%	80294	3068P-1-204	88-20-560	1	
		R22, R23	. . Res. fxd. metflm. 27.4K 1/8W 1%	75042	MEA T9 27.4K 1%	83-07-560	2	
			Schematic (reference)	00116		115-148		
			. Ohms Attenuator Board Assy	00116		115-142-83	1	
			. . Res. Mtg. Bracket #1	00116		115-418-30	1	
			. . Res. Mtg. Bracket #2	00116		115-419-30	1	
			. . Res. Mtg. Rod, long	00116		115-420-30	1	
			. . Res. Mtg. Rod, short	00116		115-421-30	1	
		CR8 thru CR22	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	15	
		K21 thru K26	. . Relay, 12V 960 ohms 1 amp Coil Nom	A1000	342-1A	82-77-100	6	
		R29, R30	. . Res. fxd. comp. 3.9K 1/4W 5%	01121	CB3925	86-04-424	2	
		R31, R33	. . Res. fxd. comp. 3Ω 1/4W 5%	01121	CB3001	86-04-112	2	
		R32, R35	. . Res. fxd. comp. 300Ω 1/4W 5%	01121	CB3015	86-04-312	2	
		R34, R36, R37, R38, R141	. . Res. Variable 10K 1/2W 10%	80294	3067P-1-103	88-20-836	5	
		R39, R40	. . Res. fxd. WW SET 9K, 1001Ω 1/2W .05%	00116		12-25-810	1	
		R41	. . Res. fxd. WW 1K 1/2W .01%	00116		12-26-079	1	
		R42	. . Res. fxd. comp. 100K 1/4W 5%	01121	CB1045	86-04-564	1	
		R43	. . Res. fxd. WW 10K 1/2W .01%	00116		12-26-128	1	
		R44, R48	. . Res. fxd. comp. 2 meg 1/4W 5%	01121	CB2055	86-04-692	2	
		R45	. . Res. fxd. WW 100K 1/2W .01%	00116		12-26-272	1	
		R46	. . Res. fxd. comp. 200K 1/4W 5%	01121	CB2045	86-04-592	1	
		R47, R49	. . Res. fxd. WW 1 meg 1/2W .01%	00116		12-26-616	2	
		R50	. . Res. fxd. comp. 2.2 meg 1/4W 5%	01121	CB2255	86-04-696	1	
			Schematic (reference)	00116		115-148		

REFERENCES FIG	REFERENCES IND	REFERENCES SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. Ohms Board Assy	00116		115-146-80	1	
			. . Handle	00116		00-36-024B	1	
			. . Shield	00116		115-411-30	1	
			. . Connector Mtg. Bar	00116		115-412-30	1	
			. . Connector, Coaxial	71785	235-09-00-101	70-20-208	1	
			(Mating Connector)	71785	236-09-00-101	70-20-210	1	
			. . Connector, 12 pin	71785	250-12-30-170	70-20-221	1	
			. . Connector, Coaxial Insert	71785	318-11-99-210	70-20-214	2	
			. . Angle Bracket	72653	6261	74-08-001	2	
			. . Cap. fxd. durmica .001μF 500V	04062	DM-15-102J	53-01-102	1	
			. . Cap. fxd. poly. .047μF 100V	12406	PD1A-473K	60-01-473	1	
			. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	1	
			. . Relay	09026	BR16-190-B-11-12-V	82-10-015	1	
			. . Res. fxd. comp. 100Ω 1/4W 5%	01121	CB1015	86-04-264	1	
			. . Res. fxd. comp. 10K 1/4W 5%	01121	CB1035	86-04-464	1	
			. . Res. fxd. comp. 100K 1/4W 5%	01121	CB1045	86-04-564	2	
			. . Res. fxd. comp. 200Ω 1/2W 5%	01121	EB2015	86-05-292	1	
			. . Res. fxd. comp. 2K 1/2W 5%	01121	EB2025	86-05-392	2	
			. . Res. fxd. comp. 10K 1/2W 5%	01121	EB1035	86-05-464	1	

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. AC-1 Converter Board Assy	00116		115-144-85	1	
			. . Top Attenuator Shield	00116		115-416-33	1	
			. . Bottom Attenuator Shield	00116		115-430-30	1	
			. . End Shield	00116		115-415-31	1	
			. . Handle	00116		00-26-024B	1	
			. . Transistor Heatsink	00116		115-417-30	1	
			. . Transistor Heatsink	00116		115-437-30	1	
		C1, C8, C34, C37, C39	. . Cap. fxd. cer. .01μF 50V	56289	19C214A6	45-05-112	5	
		C2	. . Cap. fxd. ta. 6.8μF 6V	56289	150D685X0006A2	64-00-685	1	
		C3	. . Cap. fxd. poly. .1μF 100V	12406	PD1A-104F	60-01-105	1	
		C4, C5, C7, C13, C14	. . Cap. fxd. metmy. .01μF 200V	12406	ZX2A-103K	55-00-103	5	
		C6, C9, C11, C26	. . Cap. fxd. cer. .001μF 1000V	71590	DD-102	48-10-102	5	
		C10, C12, C25	. . Cap. fxd. durmica 1000μμF 500V	04062	DM-15-102J	53-01-102	3	
		C15, C29	. . Cap. Variable Glass .8-23μμF	73899	VC-32GW	65-00-035	2	
		C16	. . Cap. fxd. durmica 10μμF 500V	04062	DM-15-100J	53-01-100	1	
		C17, C18	. . Cap. fxd. durmica 2μμF 500V	04062	DM-15-020K	53-00-020	2	
		C19, C28	. . Cap. fxd. durmica 5μμF 500V	04062	DM-15-050K	53-00-050	2	
		C20	. . Cap. Variable Glass .8-8.5μμF	73899	VC-9GW	65-00-005	1	
		C21, C22	. . Cap. fxd. durmica 1μμF 500V	04062	DM-10-010	53-02-010	2	
		C23, C24	. . Cap. fxd. durmica 100μμF 500V	04062	DM-15-101J	53-01-101	2	
		C30	. . Cap. fxd. durmica 390μμF 500V	04062	DM-15-391J	53-01-391	1	
		C31	. . Cap. fxd. cer. 820μμF 1000V	71590	DD-821	48-10-821	1	
		C32, C33	. . Cap. fxd. ta. 220μF 6V	06751	TS4K-6-227	64-21-227	2	
		C36	. . Cap. fxd. durmica 510μμF 500V	04062	DM-15-511G	53-01-511	1	
		C41	. . Cap. fxd. metmy. .022μF 200V	12406	ZX2A-223K	55-00-223	1	
		C35, C38	. . SOT					
		CR1 thru CR4, CR8 thru CR11, CR42	. . Semicon. Device, Diode spec. no. 43224	00116		94-43-224	9	
		CR5, CR12, CR20, CR35, CR38, CR39	. . Semicon. Device, Diode spec. no. 001-581-00	00116		94-45-581	6	
		CR6, CR7, CR15, CR16, CR17, CR18, CR22, CR23, CR25, CR26, CR27, CR29, CR32, CR40, CR41	. . Semicon. Device, Diode	73293	1N456	92-04-560	15	
		CR13, CR14, CR28, CR37	. . Semicon Device, Diode	07910	1N754A	92-07-541	4	

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. AC-1 Converter Board Assy (cont)					
		CR19	. . Semicon, Device, Diode	81483	1N968B	92-09-685	1	
		CR21	. . Semicon, Device, Diode	81483	1N963B	92-09-633	1	
		CR30, CR31 CR33, CR34	. . Semicon. Device, Diode	09213	1N916	92-09-160	4	
		K1, K2	. . Reed Relay, Coil spec. no. 105-514-02	00116		82-73-027	2	
		K1, K2	. . Reed Relay spec. no. 011-018-00	00116		82-73-202	2	
		K3	. . Reed Relay	15636	Type 202-2	82-73-001	1	
		Q1, Q16, Q37, Q40, Q43	. . Transistor, si. NPN	09213	2N2714	91-27-140	5	
		Q2, Q17	. . Transistor, Si. PNP	07263	2N3638	91-36-380	2	
		Q3, Q41	. . Transistor, Si. NPN	49671	40053	94-65-053	2	
		Q4, Q5, Q6, Q8, Q12, Q14, Q21, Q24, Q26, Q34 Q38	. . Transistor, Si. NPN	09213	2N3391	91-33-910	11	
		Q7-Q11, Q20-Q29, Q25-Q33	. . Transistor, Matched Set spec. no. 011-021-00	00116		94-58-601	3	
		Q9, Q18, Q27	. . Transistor spec. no. 001-517-00	00116		94-58-518	3	
		Q10A-Q10B, Q19A-Q19B, Q31A-Q31B	. . Transistor, Dual Differential spec. no. 001-513-00	00116		94-60-230	3	
		Q15, Q39, Q42	. . Transistor, Si, NPN spec. no. 001-515-00	00116		94-60-200	3	
		Q23A-Q23B	. . Transistor, Dual Differential spec. no. 001-514-00	00116		94-60-240	1	
		Q30	. . Transistor, Si. PNP	07263	2N3640	91-36-400	1	
		Q35, Q36	. . Transistor, Si. NPN	09213	2N3390	91-33-900	2	
		R1, R16, R17, R32, R96, R101, R112, R128	. . Res. fxd. comp. 10K 1/4W 5%	01121	CB1035	86-04-464	10	
		R2, R41, R42, R102, R103	. . Res. fxd. comp. 1K 1/4W 5%	01121	CB1025	86-04-364	5	
		R3	. . Res. fxd. comp. 180K 1/4W 5%	01121	CB1845	86-04-588	1	
		R4, R24, R51, R117	. . Res. fxd. comp. 22K 1/4W 5%	01121	CB2235	86-04-496	4	
		R5, R13	. . Res. fxd. comp. 1K 1W 5%	01121	GB1025	86-06-364	2	
		R6, R8, R35, R52	. . Res. fxd. comp. 1 meg 1/4W 5%	01121	CB1055	86-04-664	4	
		R7	. . Res. fxd. comp. 7.5K 1/4W 5%	01121	CB7525	86-04-452	1	
		R9, R63	. . Res. fxd. comp. 390K 1/4W 5%	01121	CB3955	86-04-624	2	
		R10, R29, R45, R64, R93, R106	. . Res. fxd. comp. 150Ω 1/4W 5%	01121	CB1515	86-04-280	6	
		R11, R46, R65, R107	. . Res. fxd. comp. 300Ω 1/4W 5%	01121	CB3015	86-04-312	4	
		R12, R70, R79, R81, R117	. . Res. fxd. comp. 100Ω 1/4W 5%	01121	CB1015	86-04-264	5	
		R14, R15, R125, R126	. . Res. fxd. metflm. 249K 1/8W	75042	MEA T9 249K 1%	83-07-824	4	

REFERENCES FIG	IND	SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. AC-1 Converter Board Assy (cont)					
		R18, R19, R119, R120	. . Res. Variable 200K 1/5W 20%	80294	3068P-1-204	88-20-966	4	
		R21	. . Res. fxd. comp. 8.2 meg 1/4W 5%	01121	CB8265	86-04-755	1	
		R22, R43, R104	. . Res. fxd. comp. 680K 1/4W 5%	01121	CB6855	86-04-648	3	
		R23	. . Res. fxd. comp. 120K 1/4W 5%	01121	CB1245	86-06-572	1	
		R25	. . Res. fxd. comp. 1.1K 1W 5%	01121	GB1125	86-06-638	1	
		R26	. . Res. fxd. comp. 2.2 meg 1/4W 5%	01121	CB2255	86-04-696	1	
		R27, R39, R40, R72, R91	. . Res. fxd. metflm. 200K 1/4W 1%	75042	MEB T9 200K 1%	83-37-730	5	
		R28, R30, R84, R86, R92, R94, R97	. . Res. fxd. comp. 4.7K 1/4W 5%	01121	CB4725	86-04-432	7	
		R31, R113, R127	. . Res. fxd. comp. 82Ω 1/4W 5%	01121	CB8205	86-04-256	3	
		R33, R62, R71	. . Res. fxd. comp. 2.2K 1/4W 5%	01121	CB2225	86-04-396	3	
		R34, R36, R56	. . Res. fxd. comp. 15K 1/5W 5%	01121	CB1535	86-04-480	3	
		R37	. . Res. fxd. comp. 75Ω 1/4W 5%	01121	CB7505	86-04-252	1	
		R38	. . Res. fxd. comp. 1.5K 1/4W 5%	01121	CB1525	86-04-380	1	
		R44, R105	. . Res. fxd. comp. 39K 1/4W 5%	01121	CB3935	86-04-524	2	
		R47, R55, R57, R82, R83, R100	. . Res. , fxd. comp. 100K 1/4W 5%	01121	CB1045	86-04-564	6	
		R48, R49	. . Res. fxd. comp. 39 meg 1/4W 5%	01121	CB3965	86-04-816	2	
		R50	. . Res. fxd. comp. 330K 1/4W 5%	01121	CB3345	86-04-616	1	
		R53	. . Res. fxd. comp. 510K 1/4W 5%	01121	CB5145	86-04-636	1	
		R54	. . Res. fxd. comp. 68K 1/4W 5%	01121	CB6835	86-04-584	1	
		R58, R59, R75, R76	. . Res. fxd. metflm. 100K 1/8W 1%	75042	MEA T9 100K 1%	83-07-780	4	
		R60, R61	. . Res. fxd. comp. 5.1K 1/4W 5%	01121	CB5125	86-04-436	2	
		R66, R74	. . Res. fxd. WW SET 990K, 10.101K 1/4W .02%	00116		15-13-515	1	
		R67	. . Res, fxd. metflm. 1 meg 1/2W 1%	75042	MEC T9 1 meg. 1%	83-59-900	1	
		R68	. . Res. fxd. metflm. 499K 1/8W .1%	75042	MEA T9 499K . 1%	83-27-900	1	
		R69, R123	. . Res. Variable 10K 1/2W 10%	80294	200P-1-103	88-20-770	2	
		R77, R78	. . Res. fxd. metflm. 500Ω 1/8W 1%	75042	MEA T8 500Ω 1%	83-05-329	2	
		R80	. . Res. fxd. comp. 2.7K 1/4W 5%	01121	CB2725	86-04-408	1	
		R85	. . Res. fxd. comp. 2.4K 1/4W 5%	01121	CB2425	86-04-404	1	
		R87, R90	. . Res. fxd. comp. 4.7 meg 1/4W 5%	01121	CB4755	86-04-732	2	
		R88, R89	. . Res. fxd. metflm. 10K 1/4W .1%	75042	MEB T9 10K . 1%	83-37-525	2	
		R94	. . Res. fxd. comp. 560K 1/4W 5%	01121	CB5645	86-04-640	1	
		R95	. . Res. fxd. comp. 51K 1/4W 5%	01121	CB5135	86-04-536	1	
		R98	. . Res. fxd. comp. 3.3K 1/4W 5%	01121	CB3325	86-04-416	1	
		R99	. . Res. fxd. comp. 3K 1/4W 5%	01121	CB3025	86-04-412	1	

REFERENCES FIG	REFERENCES IND	REFERENCES SCHEMATIC	DESCRIPTION 1 2 3 4 5 6 7	MANUFACTURER'S CODE	MANUFACTURER'S PART NO.	HONEYWELL PART NO.	QTY/ ASSY	EFF. CODE
			. AC-1 Converter Board Assy (cont)					
		R108	. . Res. fxd. metflm. 54. 9K 1/8W . 1%	75042	MEA T9 54. 9K . 1%	83-27-727	1	
		R109	. . Res. Variable 1K 1/2W 10%	80294	200P-1-102	88-20-495	1	
		R111	. . Res. fxd. metflm. 464Ω 1/8W . 1%	75042	MEA T9 464Ω . 1%	83-27-314	1	
		R114	. . Res. fxd. comp. 200Ω 1/4W 5%	01121	CB2015	86-04-292	1	
		R115	. . Res. fxd. comp. 1. 5K 1W 5%	01121	GB1525	86-06-380	1	
		R118	. . Res. fxd. comp. 220K 1/4W 5%	01121	CB2245	86-04-596	1	
		R121	. . Res. fxd. comp. 56K 1/4W 5%	01121	CB5635	86-04-540	1	
		R122	. . Res. fxd. metflm. 499K 1/8W 1%	75042	MEA T9 499K 1%	83-07-900	1	
		R124	. . Res. fxd. comp. 3. 9 meg 1/4W 5%	01121	CB3955	86-04-725	1	
		R130	. . Res. fxd. comp. 510Ω 1/4W 5%	01121	CB5115	86-04-336	1	
			Schematic (reference)	00116		115-144		


100417